User's Manual

KPCI-3108 Series
PCI Bus Data Acquisition Boards

KEITHLEY

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KPCI-3108 Series
PCI Bus Data Acquisition Boards
User's Manual

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Manual Print History

The print history shown below lists the printing dates of all Revisions and Addenda created for this manual. The Revision Level letter increases alphabetically as the manual undergoes subsequent updates. Addenda, which are released between Revisions, contain important change information that the user should incorporate immediately into the manual. Addenda are numbered sequentially. When a new Revision is created, all Addenda associated with the previous Revision of the manual are incorporated into the new Revision of the manual. Each new Revision includes a revised copy of this print history page.

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All Keithley product names are trademarks or registered trademarks of Keithley Instruments, Inc.
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Safety Precautions

The following safety precautions should be observed before using this product and any associated instrumentation. Although some instruments and accessories would normally be used with non-hazardous voltages, there are situations where hazardous conditions may be present.

This product is intended for use by qualified personnel who recognize shock hazards and are familiar with the safety precautions required to avoid possible injury. Read the operating information carefully before using the product.

The types of product users are:

Responsible body is the individual or group responsible for the use and maintenance of equipment, for ensuring that the equipment is operated within its specifications and operating limits, and for ensuring that operators are adequately trained.

Operators use the product for its intended function. They must be trained in electrical safety procedures and proper use of the instrument. They must be protected from electric shock and contact with hazardous live circuits.

Maintenance personnel perform routine procedures on the product to keep it operating, for example, setting the line voltage or replacing consumable materials. Maintenance procedures are described in the manual. The procedures explicitly state if the operator may perform them. Otherwise, they should be performed only by service personnel.

Service personnel are trained to work on live circuits, and perform safe installations and repairs of products. Only properly trained service personnel may perform installation and service procedures.

Exercise extreme caution when a shock hazard is present. Lethal voltage may be present on cable connector jacks or test fixtures. The American National Standards Institute (ANSI) states that a shock hazard exists when voltage levels greater than 30V RMS, 42.4V peak, or 60VDC are present. **A good safety practice is to expect that hazardous voltage is present in any unknown circuit before measuring.**

Users of this product must be protected from electric shock at all times. The responsible body must ensure that users are prevented access and/or insulated from every connection point. In some cases, connections must be exposed to potential human contact. Product users in these circumstances must be trained to protect themselves from the risk of electric shock. If the circuit is capable of operating at or above 1000 volts, **no conductive part of the circuit may be exposed.**

As described in the International Electrotechnical Commission (IEC) Standard IEC 664, digital multimeter measuring circuits (e.g., Keithley Models 175A, 199, 2000, 2001, 2002, and 2010) are Installation Category II. All other instruments' signal terminals are Installation Category I and must not be connected to mains.

Do not connect switching cards directly to unlimited power circuits. They are intended to be used with impedance limited sources. NEVER connect switching cards directly to AC mains. When connecting sources to switching cards, install protective devices to limit fault current and voltage to the card.

Before operating an instrument, make sure the line cord is connected to a properly grounded power receptacle. Inspect the connecting cables, test leads, and jumpers for possible wear, cracks, or breaks before each use.

For maximum safety, do not touch the product, test cables, or any other instruments while power is applied to the circuit under test. ALWAYS remove power from the entire test system and discharge any capacitors before: connecting or disconnecting cables or jumpers, installing or removing switching cards, or making internal changes, such as installing or removing jumpers.

Do not touch any object that could provide a current path to the common side of the circuit under test or power line (earth) ground. Always make measurements with dry hands while standing on a dry, insulated surface capable of withstanding the voltage being measured.

The instrument and accessories must be used in accordance with its specifications and operating instructions or the safety of the equipment may be impaired.

Do not exceed the maximum signal levels of the instruments and accessories, as defined in the specifications and operating information, and as shown on the instrument or test fixture panels, or switching card.

When fuses are used in a product, replace with same type and rating for continued protection against fire hazard.

Chassis connections must only be used as shield connections for measuring circuits, NOT as safety earth ground connections.

If you are using a test fixture, keep the lid closed while power is applied to the device under test. Safe operation requires the use of a lid interlock.

If a screw is present, connect it to safety earth ground using the wire recommended in the user documentation.

The symbol on an instrument indicates that the user should refer to the operating instructions located in the manual.

The symbol on an instrument shows that it can source or measure 1000 volts or more, including the combined effect of normal and common mode voltages. Use standard safety precautions to avoid personal contact with these voltages.

The **WARNING** heading in a manual explains dangers that might result in personal injury or death. Always read the associated information very carefully before performing the indicated procedure.

The **CAUTION** heading in a manual explains hazards that could damage the instrument. Such damage may invalidate the warranty.

Instrumentation and accessories shall not be connected to humans.

Before performing any maintenance, disconnect the line cord and all test cables.

To maintain protection from electric shock and fire, replacement components in mains circuits, including the power transformer, test leads, and input jacks, must be purchased from Keithley Instruments. Standard fuses, with applicable national safety approvals, may be used if the rating and type are the same. Other components that are not safety related may be purchased from other suppliers as long as they are equivalent to the original component. (Note that selected parts should be purchased only through Keithley Instruments to maintain accuracy and functionality of the product.) If you are unsure about the applicability of a replacement component, call a Keithley Instruments office for information.

To clean an instrument, use a damp cloth or mild, water based cleaner. Clean the exterior of the instrument only. Do not apply cleaner directly to the instrument or allow liquids to enter or spill on the instrument. Products that consist of a circuit board with no case or chassis (e.g., data acquisition board for installation into a computer) should never require cleaning if handled according to instructions. If the board becomes contaminated and operation is affected, the board should be returned to the factory for proper cleaning/servicing.

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1
Overview

Preface

This manual is provided for persons needing to understand the installation, interface requirements, functions, and operation of the KPCI-3108 Series boards. The KPCI-3108 provides two 16-bit analog outputs; the KPCI-3107 does not provide analog outputs.

NOTE *Unless noted otherwise—in situations discussing analog outputs—this manual refers to both models collectively as KPCI-3108.*

This manual focuses primarily on describing the KPCI-3108 Series boards and their capabilities, setting up the boards and their associated software, making typical hookups, and troubleshooting. There are also sections that discuss calibration and summarize characteristics of DriverLINX test panel software.

To follow the information and instructions contained in this manual, you must be familiar with the operation of Windows 95, 98, or NT, with basic data-acquisition principles, and with your application. However, if you find unfamiliar terms in this manual, check the glossary in Appendix B. To locate topics discussed in this manual, search the index.

To use this manual effectively, review the remaining brief topics in this preface:

- The organization of the manual
- The special font/typeface conventions used in the manual
- Moving quickly to cross-referenced parts of the manual (in the electronic [PDF] version).

The remainder of Section 1 summarizes general hardware characteristics of the KPCI-3108 board, computer system requirements to run the board, and software and accessories that can be used with the board.

How the manual is organized

The KPCI-3108 User's Manual is organized as follows:

- Section 1 describes general features and system requirements and summarizes supporting software and accessories for the KPCI-3108 boards.
- Section 2 describes operating features of the boards in more detail. This section contains a block diagram and brief descriptions of the features as they relate to setting up and using the board.
- Section 3 contains software descriptions and installation notes and instructions for the following: inspecting the board, installing the board, checking the board and software installation, installing accessories, and connecting signals.
- Section 4 summarizes the test panels that are available in the DriverLINX software.
- Section 5 discusses how to calibrate your board using the DriverLINX calibration utility.
- Section 6 contains detailed procedures for isolating problems with your data acquisition system. This section also contains instructions for obtaining technical support.
- Appendix A contains specifications for the KPCI-3108 boards.
- Appendix B is a glossary that includes key terms used in this manual.
- A detailed index completes this manual.

How to distinguish special text items

Italic, bold, and upper-case letters, the Courier font, and quotation marks distinguish certain text items from the general text. The following text conventions are used (exclusive of headings):

- **10 point Times Bold** distinguishes the following:
  - All Windows 96/98/NT user-interaction items: commands, screen messages, menu names, menu options, and dialog-box items—including captions, user selections, and typed user inputs (but not including dialog box names, which are in regular text)
  - ***CAUTION*** statements
- *10 point Times Italic* distinguishes the following:
  - Emphasis in general
  - Cross-references to other documents, such as other manuals or books
  - *NOTE* statements
- 10 POINT TIMES UPPER CASE distinguishes the following
  - Switches, such as ON and OFF
  - Keyboard keys, such as ENTER
- `10 point Courier` distinguishes software code statements
- "Double quote marks" distinguish the following:
  - Cross references to other manual sections/chapters, such as "Troubleshooting"
  - Literals, such as the "Analog" and "Digital" labels on I/O connectors.

How to move around the electronic version of the manual

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- Mouse-click the top margin of any page to jump to the Table of Contents.
- Mouse-click on any Index or Table of Contents (TOC) page number to jump to the page.
- Mouse-click on any of these cross references to jump to the cross-referenced figure, table, section, or step (cross references are not framed in red — in contrast to the Index and Table of Contents page numbers):
  - Figure number headings, such as Figure 2-3
  - Table number headings, such as Table 1-2
  - Section/chapter headings that are enclosed in quotes, such as "System requirements"
  - Step or substep numbers/letters of a specific procedure, such as the "6" in "step 6" or such as the "g" in "substep g" or "step 6g"

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To *return* from the referenced item to what you were reading *before* you jumped to the referenced item — the Index, TOC, top page margin, or cross reference — do either of the following:

- Hold down the CONTROL key and press the [-] key (i.e. press CONTROL + -)
- In the Acrobat Reader **View** menu, click **Go Back**.

Hardware characteristics

The KPCI-3108 series boards are high-performance PCI-bus data acquisition boards for PC-compatible computers running Windows 95, 98, or NT. PCI-bus data acquisition boards, such as the KPCI-3108, have two major advantages over ISA-bus data acquisition boards:

- The PCI-bus Plug and Play feature allows a user to install the data acquisition board without making manual system configurations. Upon system power-up or reset, the PCI-bus Plug and Play feature automatically configures the board for your system, eliminating the need to set DIP switches on the board.
- Cleaner, faster, direct data transfer to and from memory via bus mastering, bypassing the CPU.
  - Data transfer occurs at speeds up to 132 MB/sec rate for the PCI bus, versus 8.33 MB/sec maximum for the ISA bus, due to the 32 bit width and 33 MHz clock speed of the PCI bus.
  - Data transfer causes minimal interruptions to normal processing.

Major features of KPCI-3108 boards include the following:

- The following analog input characteristics:
  - Software-configurable for 16 single-ended analog input channels, eight differential analog input channels, or an intermediate number of mixed single-ended and differential analog input channels.
  - Software-configurable individual gains for each analog input channel as follows: 1, 2, 4, 8, 10, 20, 40, 80, 100, 200, 400, and 800.
  - Analog data conversion speeds up to 100 ksamples/s with 16-bit resolution.
  - A 256-location scan queue that supports high-speed sampling of analog input channels in any desired combination and sequence. The following properties may be specified for each channel in the queue: any of the available gains, either input polarity (bipolar or unipolar), and either single-ended or differential input.
  - A 2048 sample FIFO (First In First Out) data buffer for the A/D converter that ensures data integrity at high sampling rates.
  - The capability to start and stop analog-to-digital data conversions with digital hardware triggers and gates.
  - An analog about-trigger acquisition mode—the capability to stop analog-to-digital conversions after a fixed number of scans following an analog trigger.
  - Software-selectable edge-polarity detection for hardware trigger and gate signals.
- Two analog outputs from two independent 16-bit DACs (Digital-to-Analog Converters).
- A total of 32 bits of general-purpose digital I/O having high-current output capabilities. This digital I/O is divided into four registers. The 8 bits of each register may be configured as all inputs or all outputs.
- A total of 12 bits of multi-function digital I/O, six input bits and six output bits.
  The six multi-function input bits are user-configurable for different purposes, including the following:
  - Counter/timer timebase and gate inputs
  - External pacer for A/D or D/A conversion
  - External digital trigger
  - Target-mode digital input

- The six multi-function output bits are user-configurable for different purposes, including the following:
  - Counter/timer outputs
  - Trigger output
  - Pacer-clock output
  - Control and/or addressing for EXP-1800 expansion accessories or MB-02 signal conditioning accessories
  - Target-mode digital output
- Three 16-bit counter/timers, each of which is user-accessible and user-configurable
- Optional target-mode (pass-through) data transfer capability in addition to bus mastering. Both target-mode data transfer, which is sometimes referred to as pass-through operation, and bus mastering data transfer are software-configurable. To maximize the speed of analog I/O, the KPCI-3108 boards normally implement the bus mastering mode. The target mode provides a simple access port to the PCI bus for digital I/O.
- Very fast board control via a field-programmable gate array (FPGA) instead of a microprocessor. (Refer to the glossary in Appendix B for more information about FPGAs).
- Software-only calibration of analog I/O; no potentiometers to adjust.
- Two miniature 36-pin I/O connectors that require only one slot on the rear panel of the PC. These connect to other equipment via standard, readily available interface cables that are shielded and transmit signals through twisted pairs.

For more detailed information on these features, refer to Section 2, "Functional Description."

Specifications

General specifications are listed in Appendix A. I/O connections are identified in Section 3 and Appendix B.

System requirements

The system capabilities required to run the KPCI-3108 board, and to use the DriverLINX software supplied with the board, are listed in Table 1-1.

Table 1-1
System requirements

CPU Type	Pentium or higher processor on motherboard with PCI bus version 2.1
Operating system	Windows 95 or 98
	Windows NT version 4.0 or higher
Memory	16 MB or greater RAM when running Windows 95 or 98
	32 MB or greater RAM when running Windows NT
Hard disk space	4 MB for minimum installation
	50 MB for maximum installation
Other	A CD-ROM drive*
	A free PCI-bus expansion slot capable of bus mastering
	Enough reserve computer power supply capacity to power the KPCI-3108 Series board, which draws 0.8A at 5VDC and 0.5A at +12VDC.

* Any CD-ROM drive that came installed with the required computer should be satisfactory. However, if you have post-installed an older CD-ROM drive or arrived at your present system by updating the microprocessor or replacing the motherboard, some early CD-ROM drives may not support the long file names often used in 32 bit Windows files.

Software

The user can select a fully integrated data acquisition software package such as TestPoint or LabVIEW or write a custom program supported by DriverLINX.

DriverLINX is the basic Application Programming Interface (API) for the KPCI-3108 boards:

- It supports programmers who wish to create custom applications using Visual C/C++, Visual Basic, or Delphi.
- It accomplishes foreground and background tasks to perform data acquisition.
- It is the needed interface between TestPoint and LabVIEW and a KPCI-3108 board.

DriverLINX software and user's documentation on a CD-ROM are included with your board.

TestPoint is an optional, fully featured, integrated application package with a graphical drag-and-drop interface which can be used to create data acquisition applications without programming.

LabVIEW is an optional, fully featured graphical programming language used to create virtual instrumentation.

Refer to Section 3, "lnstallation," for more information about DriverLINX, TestPoint, and LabView.

Accessories

Accessories available to interface your KPCI-3108 board to external circuits are listed in Table 1-2, Table 1-3, and Table 1-4.

Table 1-2
Channel-expansion, signal conditioning, and digital I/O accessories

Accessory*	Description
EXP-1800	Expansion accessory. Expands one KPCI-3108 single-ended analog input channel into 16 differential analog input channels.
MB-01	Signal-conditioning module rack. Accommodates up to 16 MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.
MB-05	Signal-conditioning module rack. Accommodates up to eight MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.
STA-MB	Signal-conditioning module box/screw-terminal accessory. Accommodates up to four MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.
MB-02	Signal-conditioning module/channel-expansion rack. Accommodates up to 16 MB Series modules. All 16 modules are multiplexed to one single-ended analog input channel of a KPCI-3108 board.
PB-24	Industry-standard relay baseboard. Accommodates 24 standard-size solid-state relay modules. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.
PB-24SM	Industry-standard relay baseboard. Accommodates 24 miniature SM Series solid-state relay modules. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.
SSIO-24	Module interface board that holds up to 24 miniature, optically-isolated solid-state digital I/O modules. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.
ERB-24	Relay board with 24 double-pole, double-throw (dual Form C) electromechanical relays. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.
SRA-01	Module interface board, in box, that holds up to eight industry-standard solid-state digital I/O modules. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.
ERA-01	Relay board, in box, with eight single-pole, double-throw (Form C) electromechanical relays. Each module is connected to one general-purpose digital output bit of a KPCI-3108 board.

*Connecting one of these accessories to a KPCI-3108 board requires an interface accessory and suitable cables. Select the required accessories and cables using one of the following figure-table combinations in Section 3: Figure 3-7 and Table 3-4, Figure 3-8 or Figure 3-9 and Table 3-6, Figure 3-10 and Table 3-8, or Figure 3-11 and Table 3-10.

Table 1-3
Screw-terminal accessories and adapter/screw-terminal accessories

Accessory*	Description
STP-36	Screw-terminal accessory. Interfaces either the "Analog" or the "Digital" KPCI-3108 Series I/O connector to screw-terminals that are numbered identically to the connector pins.
STP-36/C	An STP-36 with an added plastic frame that permits DIN-rail mounting.
STA-3108-A1	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 Series I/O connector to an EXP-1800 channel-expansion accessory, as well as to screw-terminals that are numbered identically to the "Analog" connector pins. If needed, one STA-3108 accessory can interface the KPCI-3108 to an entire daisy chain of EXP-1800 accessories. The daisy chain may contain up to sixteen EXP-1800 accessories.
STA-3108-A2	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 Series I/O connector to MB-01, MB-05, and STA-MB signal-conditioning accessories, as well as to screw-terminals that are numbered identically to the "Analog" connector pins.
STA-3108-A3	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 I/O connector to as many as four MB-02 accessories, as well as to screw-terminals that are numbered identically to the "Analog" connector pins. A daisy-chain of up to four STA-3108-A3 accessories interfaces the "Analog" KPCI-3108 I/O connector to as many as 16 MB-02 accessories.
STA-3108-D1	Adapter/screw-terminal accessory. Interfaces the "Digital" KPCI-3108 Series I/O connector to a PB-24, PB-24SM, ERB-24, SSIO-24, SRA-01, or ERA-01 digital I/O accessory, as well as to screw-terminals that are numbered identically to the "Digital" connector pins.

*Using one of these accessories to interface a KPCI-3108 board to other accessories requires suitable cables. Select the required cables using one of the following figure-table combinations in Section 3: Figure 3-7 and Table 3-4, Figure 3-8 or Figure 3-9 and Table 3-6, Figure 3-10 and Table 3-8, or Figure 3-11 and Table 3-9.

Table 1-4
Cables used to interconnect the accessories

Accessory	Description
CAB-1284CC	IEEE 1284 Type C-C shielded mini-Centronics cable, with 18 twisted pairs. Connects a screw-terminal accessory or an adapter/screw-terminal accessory to either the "Analog" or "Digital" KPCI-3108 I/O connector, as appropriate. Also used to connect two STA-3108-A3 accessories together as part of a daisy-chain.
CAB-50/1	Ribbon cable, 18 inches long, with 50-pin headers on each end. Connects an EXP-1800 accessory to an STA-3108-A1 accessory. Also used to connect two EXP-1800 accessories together as part of a daisy-chain.
C-16MB1	Cable with a 37-pin female D-type connector on one end and a 26-pin header connector on the other end. Connects an MB-01 or MB-05 accessory to an STA-3108-A2 accessory.
C-1800	Cable with a 37-pin female D-type connector on each end. Connects an STA-MB accessory to an STA-3108-A2 accessory.
C-2600	Ribbon cable, 18 inch, with a 26-pin header connector at each end (and one in the middle, not used in KPCI-3108 configurations). Connects one MB-02 accessory to an STA-3108-A3 accessory.
CAB-SSR	Ribbon cable, 3 feet. Connects a PB-24 or PB-24SM accessory to an STA-3108-D1 accessory.
CACC-2000	Ribbon cable, 24 inches with 50-pin female connector on each end. Connects an ERB-24 or SSIO-24 accessory to an STA-3108-D1 accessory.
ADP-5037	Conversion cable with a 50-pin connector at one end and a small box, terminating in a 37-pin D-type connector, at the other end. Connects an ERA-01 or SRA-01 accessory to an STA-3108-D1 accessory.

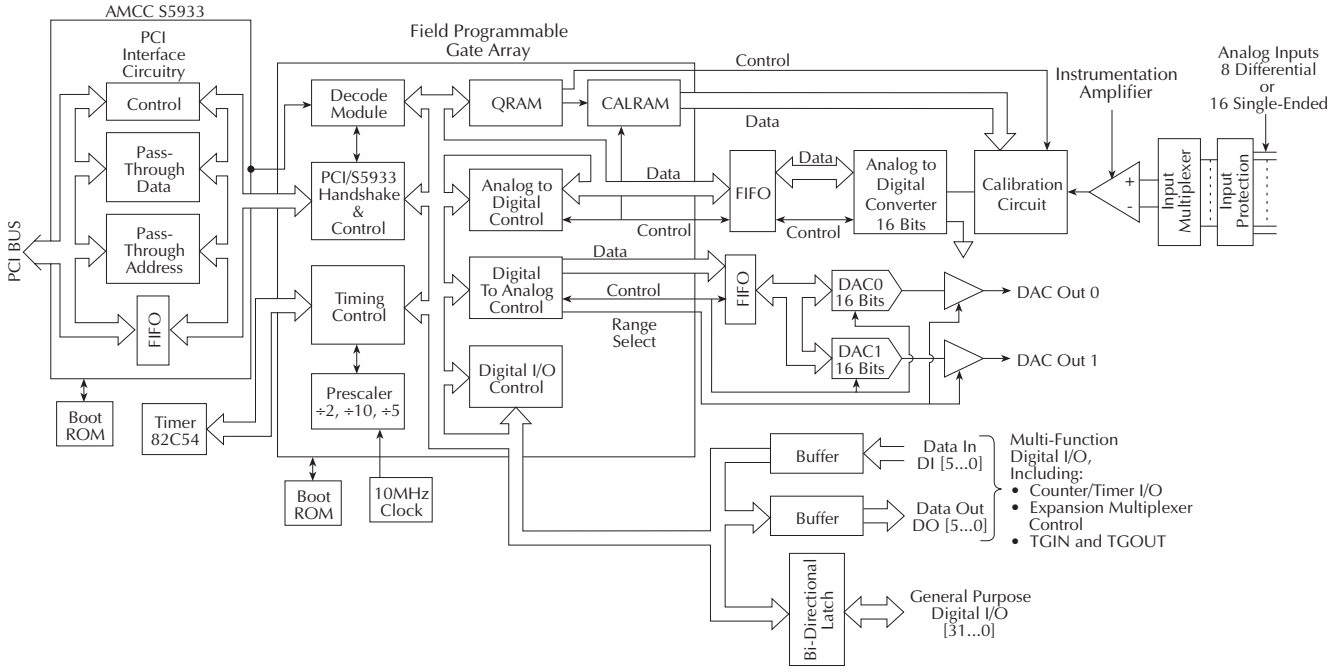
2
Functional Description

This section describes features of the following KPCI-3108 board sections: the analog inputs, the analog outputs, the general-purpose digital I/O, the multi-function digital I/O, and the counter/timers. These descriptions help familiarize you with operating options and enable you to make the best use of your board.

NOTE *Features described in this section are typically configured using custom or commercial application software which interfaces to your KPCI-3108 board via DriverLINX. For information on how to configure and apply these features, consult the appropriate manuals. Application software developers should consult your DriverLINX manuals located on the DriverLINX CD-ROM shipped with your board. Application software users should consult the manuals provided by the vendor or developer of your software.*

The block diagram in Figure 2-1 represents the KPCI-3108 Series boards.

Figure 2-1
Block diagram of KPCI-3108 board



Analog input features

This section discusses the following:

- Understanding and choosing the software-configurable analog input modes.
- Maximum data throughput specifications and tips on optimizing throughput.
- Signal conversion modes.
- Signal conversion clock sources.
- The use of triggers and gates to start and stop signal conversions.

Understanding and choosing analog input modes

Using software, you can select between various analog input options as follows:

- The differential termination mode or the single-ended termination mode.
- The unipolar input mode or the bipolar input mode.
- The input channels to be scanned to the instrumentation amplifier, in any order or combination.
- The instrumentation amplifier gain to be used.

These options may be freely mixed at each of the 256 possible steps in the scan sequence—as will be discussed in "Specifying channel number, channel gain, polarity mode, and termination mode for each position in the scan sequence."

The next four subsections, as well as the subsequent section entitled "Optimizing throughput," explain these options and provide guidance for choosing analog input modes.

Understanding the analog inputs

Each KPCI-3108 board provides 16 analog input terminals. The termination modes of these terminals—single-ended or differential—are configurable by software, as follows:

- All configured for single-ended termination mode, providing 16 input channels
- All configured for differential termination mode, providing 8 input channels
- Some configured for single-ended termination mode and others configured for differential termination mode, providing an intermediate number of input channels

NOTE *Hereafter in this manual, an input channel configured for single-ended termination mode is generally referred to as a single-ended input or single-ended channel; an input channel configured for differential termination mode is generally referred to as a differential input or differential channel.*

The characteristics of single-ended and differential inputs are as follows:

- A single-ended input measures the voltage at one input terminal relative to a common ground. A single-ended input does not reject noise and other unwanted voltages in a signal ground and does not reject a common power supply voltage, such as the excitation voltage of a bridge circuit.

  When you configure the input terminals all to be used for single-ended channels, you can connect each of the 16 input terminals to 16 external signals, maximum.

- A differential input measures the difference between the voltages at two input terminals, designated input-high and input-low. Signals at both the input-high and input-low terminals are referenced to a common ground. Differential inputs reject the common mode voltage, the voltage that each "sees" in common, except for a small fraction determined by the common mode rejection ratio (refer to the glossary in Appendix B). Differential inputs are commonly used to:
  - Reject noise and other unwanted voltages in a signal ground.
  - Reject a common power supply voltage, such as the excitation voltage of a bridge circuit.

NOTE *Refer to "Wiring analog input signals" in Section 3 for important information about wiring differential inputs.*

When you configure the input terminals all to be used for differential channels, you can connect 8 external signals, maximum, because a pair of input terminals is needed for each differential input.

- When you configure the input terminals to be used for a mixture of single-ended and differential channels, the number of available channels is less than 16 but more than 8. For example, the following configuration results in 12 available channels, maximum—4 differential channels and 8 single-ended channels:
  - You configure 4 channels as differential. Each differential channel uses 2 of the 16 input terminals. Therefore, you use 8 of the 16 input terminals for differential channels: (4 differential channels) x (2 inputs required/ differential channel) = 8 input terminals.
  - You configure 8 channels as single-ended. Each single-ended channel uses one of the 16 input terminals. Therefore, you use the other 8 of the 16 input terminals for single-ended (S.E).channels: (8 S.E. channels) x (1 input required/S.E. channel) = 8 input terminals.

Signals from all 16 input terminals are amplified by one instrumentation amplifier — a type of high performance differential amplifier — and are digitized by one 16-bit analog-to-digital converter (A/D converter or ADC). This is made possible by multiplexing, a time-sharing arrangement. Inputs are scanned and connected intermittently to the instrumentation amplifier and A/D converter according to a user-defined sequence. The inputs are connected through a pair of 8-channel multiplexers, each of which is effectively a solid-state 8-pole, single-throw switch. Additional solid-state switches connect one or both multiplexers to the instrumentation amplifier to determine whether inputs are configured for differential or single-ended termination mode.

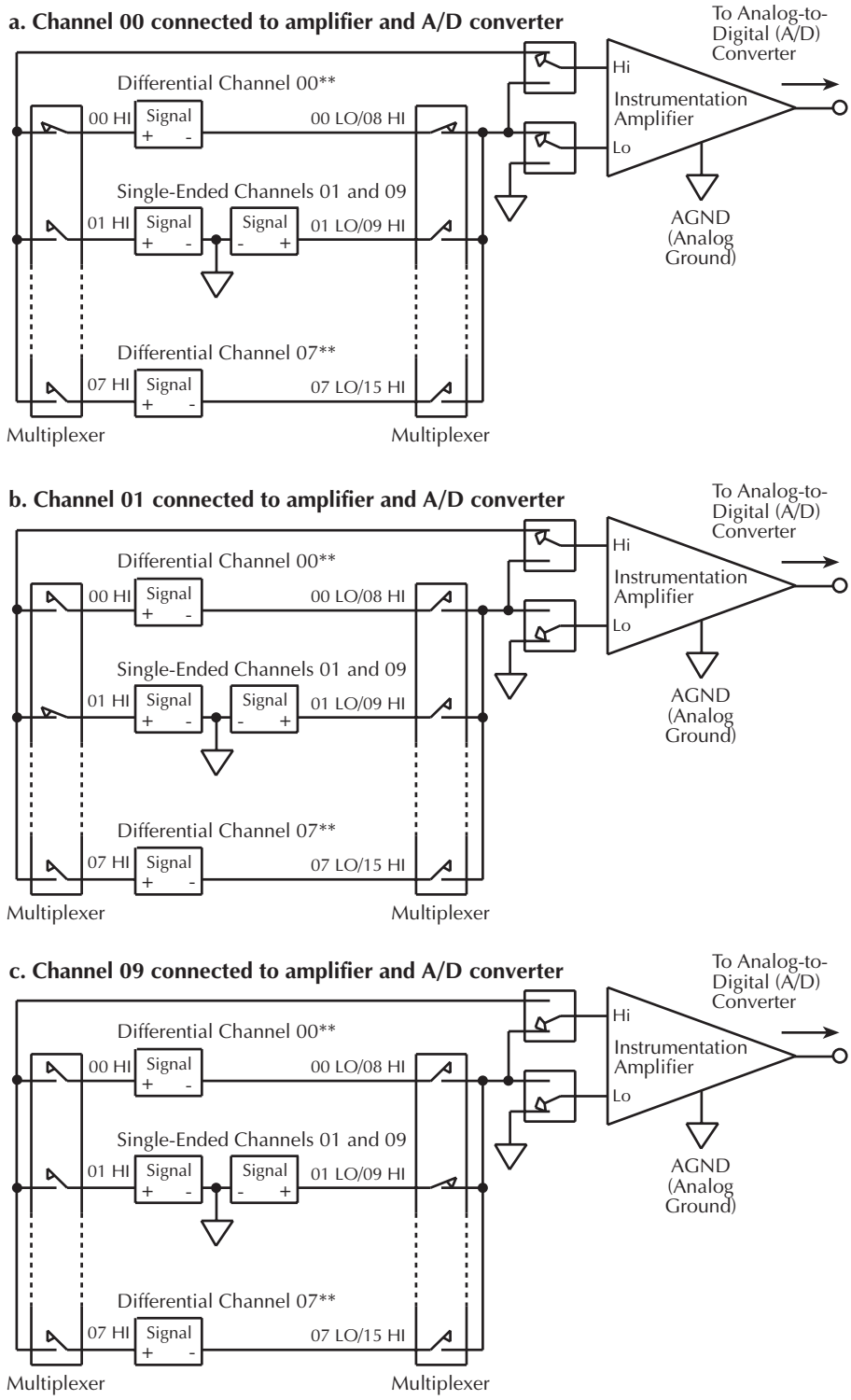
Figure 2-2 shows how a mixture of single-ended and differential channels are connected, one at a time, to the instrumentation amplifier and A/D converter. All channels of the KPCI-3108 board are connected similarly.

NOTE *The input terminal numbering in Figure 2-2 results from the need to configure all input terminals in pairs. Each pair of input terminals may be configured either for one differential channel (for example, 00 HI and 00 LO) or for two single-ended channels (01 HI and 09 LO). For additional information about channel and terminal numbering, refer to Figure 3-2, Table 3-1, Figure 3-3, and Table 3-2 in Section 3 of this manual.*

In Figure 2-2a, the board connects differential channel 00 to the amplifier and A/D converter as follows:

- The multiplexer at left and a solid-state switch connect the high-level voltage of the channel 00 signal to the input-high terminal of the instrumentation amplifier.
- The multiplexer at right and a solid-state switch connect the low-level voltage of the channel 00 signal to the input-low terminal of the instrumentation amplifier.

Figure 2-2
Multiplexing of 16 input terminals in mixed differential and single-ended termination modes



** Common-mode ground return connection required for differential inputs is not shown for simplicity.

In Figure 2-2b, the board connects differential channel 01 to the amplifier and A/D converter as follows:

- The multiplexer at left and a solid-state switch connect the high-level voltage of the Channel 01 signal to the input-high terminal of the instrumentation amplifier.
- Wiring connects the low-level voltage of the Channel 01 signal to the analog ground terminal (AGND).
- A solid-state switch connects the analog ground terminal to the input-low terminal of the instrumentation amplifier.

In Figure 2-2c, the board connects differential channel 09 to the amplifier and A/D converter as follows:

- The multiplexer at right and a solid-state switch connect the high-level voltage of the Channel 09 signal to the input-high terminal of the instrumentation amplifier.
- Wiring connects the low-level voltage of the Channel 09 signal to the analog ground terminal (AGND).
- A solid-state switch connects the analog ground terminal to the input-low terminal of the instrumentation amplifier.

In a mode not shown in Figure 2-2, solid state switches short both amplifier inputs to ground.

NOTE *The connection sequence shown in Figure 2-2 was selected for illustration purposes only. Any channel can be connected at any point in the channel scan sequence. For more information about channel sequencing, refer to "Specifying channel number, channel gain, polarity mode, and termination mode for each position in the scan sequence" later in Section 2.*

Choosing between the differential and single-ended termination modes

Generally, you should use a differential input for a low-level signal having a significant noise component and/or for a signal having a non-zero common-mode voltage. You should use a single-ended input for a high-level signal having a relatively small noise component.

There is no absolute level at which one of these input configurations becomes more effective than the other. However, you should generally use a differential input for a voltage range of 100mV or below.

Choosing between the unipolar and bipolar input modes

Using software, you can configure any KPCI-3108 input channel to operate in either the unipolar or bipolar input mode. A unipolar signal is always positive (0 to +5V, for example). A bipolar signal can swing between positive and negative values (±5V maximum, for example). For example, an unbiased sinusoidal AC signal is bipolar.

Use the bipolar mode only if you must measure signals having both positive and negative polarity. A bipolar range provides only half as good resolution as a unipolar range of the same magnitude. If your signal will always be positive (at or above 0.0V), use the unipolar mode for maximum resolution.

Resolutions for unipolar and bipolar inputs are listed in Table 2-1.

Table 2-1
Gains, ranges, and resolutions for a KPCI-3108 board

	Bipolar		Unipolar	
Gain	**Range**	**Resolution**	**Range**	**Resolution**
1	±10.0 V	305 µV	0 to +10.0 V	153 µV
2	±5.0 V	153 µV	0 to +5.0 V	76 µV
4	±2.5 V	76 µV	0 to +2.5 V	38 µV
8	±1.25 V	38 µV	0 to +1.25 V	19 µV
10	±1.0 V	31 µV	0 to +1.0 V	15 µV
20	±500 mV	15 µV	0 to +500 mV	7.6 µV
40	±250 mV	7.6 µV	0 to +250 mV	3.8 µV
80	±125 mV	3.8 µV	0 to +125 mV	1.9 µV
100	±100 mV	3.1 µV	0 to +100 mV	1.5 µV
200	±50 mV	1.5 µV	0 to +50 mV	0.8 µV
400	±25 mV	0.8 µV	0 to +25 mV	0.4 µV
800	±12.5 mV	0.4 µV	0 to +12.5 mV	0.2 µV

NOTE: Numbers are rounded for readability.

CAUTION **The board does not provide overrange detection. Each range listed in Table 2-1 represents the measured value that will be reported to the computer if your input signal voltage equals or exceeds the range. Therefore, if the range is set at ±2.5V (gain = 4) and your signal voltage is +3.1V, the measured value will be reported at +2.5V.**

Specifying channel number, channel gain, polarity mode, and termination mode for each position in the scan sequence

Using software, you can specify a list of up to 256 channel numbers, in any order or combination, to be measured sequentially each time a scan is initiated. For each position in the scan sequence you specify the following:

- The number of the channel to be measured.
- The gain to be used for that measurement.
- The polarity mode—bipolar or unipolar—to be used for that measurement.
- The termination mode—single-ended or differential—to be used for that measurement.

The entire list of sequential scan specifications is sometimes referred to as a channel gain queue. However, it specifies more than just channels and gains for a KPCI-3108 board.

Channel numbers may be skipped or be repeated in the queue if desired. For example, by repeating a channel number in the queue, you can do the following:

- Sample some channels more frequently than others.
- Provide extra settling time to wash out residual signals between gain changes.
- Provide extra samples for averaging.

Figure 2-3 illustrates a possible channel-gain queue.

Figure 2-3
Channel-gain queue example

Position in queue	1st	2nd	3rd	4th	5th	6th	7th	8th	9th	10th	-------	254th	255th	256th
Channel number	02	03	11	11	01	05	03	02	07	07	-------	13	14	02
Channel gain	40	2	4	4	40	2	1	20	200	200	-------	2	4	40
Polarity Mode*	+	+	±	±	+	±	+	+	±	±	-------	+	±	±
Termination Mode**	D	SE	SE	SE	D	SE	SE	D	D	D	-------	SE	SE	D

* Note: ± = bipolar and + = uniploar
** Note: D = differential and SE = single ended

All 256 combinations of channel, gain, polarity mode, and termination mode in the channel gain queue are held in a 256-position RAM. You need not specify combinations for all 256 positions, however.

Refer to Table 2-1 for available gains and corresponding input ranges.

Optimum selection and sequencing of channel gains may be affected by your required throughput and by noise and other stray signals. Refer to "Optimizing throughput" for general recommendations about channel-gain selection and sequencing. Refer to "Avoiding wiring problems at high gains" in Section 3 for recommendations to minimize signal errors at high gains.

Throughput

Throughput is the maximum rate at which the data acquisition board can perform repetitive conversions within a specified accuracy. Signal throughput depends on the gain settings for individual channels and for adjacent channels in the channel-gain queue. This section discusses general recommendations to optimize throughput and lists KPCI-3108 throughput for specific conditions.

Optimizing throughput

Though you can change input ranges on a per-channel basis, throughput is likely to drop if you group channels with varying gains in sequence. This throughput drop occurs for two reasons. Firstly, channels with low-level inputs (100mV or less) are inherently slower than channels with high-level inputs signals left by high-level inputs. Secondly, extra settling time is required for

low-level inputs to wash out residual signals. The best way to maximize throughput is to use a combination of sensible channel grouping and external signal conditioning. When using the channel-gain queue, consider the following suggestions:

- Put all channels that use the same range in the same group, even if you must arrange the channels out of sequence.
- To acquire low-level signals at high-speeds, preamplify the signal to the maximum input range of the board using external signal. External amplification increases total system throughput and reduces noise.
- If low-level inputs are relatively slow and high-level inputs are relatively fast, maintain two channel lists: one for slow inputs and the other for fast inputs.
- If some channels are not used, you can provide extra settling time for a channel that is used, as follows:
  - Assign two (or more) consecutive, identical channel-gain entries to this channel.
  - Ignore the measurement results from the first channel-gain entry.

  This approach allows the input signal measured through the first entry to largely wash out residuals before the same input signal is measured through the second entry.

You must take special care when directly measuring low-level signals. When using ranges of ±100mV, 0 to 100mV, or smaller, the measurement throughput drops for two reasons:

- The amplifier settles more slowly.
- Noise in the measurements is higher and therefore requires post-acquisition filtering (averaging) to achieve accurate results.

Because the KPCI-3108 has a very high bandwidth — about 1MHz for low level signals, any noise is amplified and digitized. Therefore, you must measure low-level signals carefully to minimize noise effects.

Low-level transducers are best used with signal conditioning. Always use the differential termination mode when making measurements with the ±12.5 mV, 0 to 12.5 mV, ±25 mV, 0 to 25 mV, ±100 mV, and 0 to 100 mV ranges.

Subsequent sections show throughput for various configurations. Note that these throughputs are based on driving an input with an ideal voltage source. The output impedance and drive capabilities of the source are far more critical when making large gain changes between two channels, especially when the gains are at opposite extremes of the input range. Consider the following:

- Consider the measurement of a signal near -25 mV just after measurement of a signal near +5 V. You get better performance when driving adjacent channels at the same gain.
- The source must be able to drive the input capacitance of the multiplexer and board. The input effective capacitance of a single channel of a KPCI-3108 board is 200pF, in series with approximately 1kΩ.

NOTE *The effective input capacitance, which must be charged by your signal sources, is 200pF. The series impedance between the input terminal and this capacitance is about 1kΩ. This series RC combination, along with amplifier slew rate, is a primary throughput-limiting factor. Therefore, advertised throughputs for the KPCI-3108 board are calculated assuming that the user's source impedance is substantially less than 1kΩ. Consequently, if any of your signal sources have high impedance, test the throughput for those sources while scanning the inputs. If your tests indicate reduced throughput, insert extra entries into the channel-gain queue for the high-impedance signal sources (refer to the recommendations earlier in this section). Extra scan queue entries allow extra settling time.*

Throughput for channel-to-channel sampling at fixed gain

If you are sampling at only one channel at any gain, the maximum throughput is 100 ksamples/s.

If you are sampling multiple channels at a fixed gain, the maximum throughput for channel-to-channel sampling is as listed in Table 2-2. In both cases, a 0.02% maximum error applies, assuming an ideal voltage source.

Table 2-2
Maximum throughput for channel-to-channel sampling at fixed gain

Gain	Bipolar throughput	Unipolar throughput
1	100 ksamples/s	100 ksamples/s
2	100 ksamples/s	100 ksamples/s
4	100 ksamples/s	100 ksamples/s
8	100 ksamples/s	100 ksamples/s
10	100 ksamples/s	100 ksamples/s
20	100 ksamples/s	100 ksamples/s
40	100 ksamples/s	100 ksamples/s
80	100 ksamples/s	100 ksamples/s
100	50 ksamples/s	50 ksamples/s
200	50 ksamples/s	50 ksamples/s
400	50 ksamples/s	50 ksamples/s
800	50 ksamples/s	50 ksamples/s

Data conversion modes

KPCI-3108 boards support two data-conversion modes: paced mode and burst mode. The conversion rate for each mode is controlled by an independent clock: the pacer clock for paced mode and the burst clock for burst mode.

Paced conversion mode

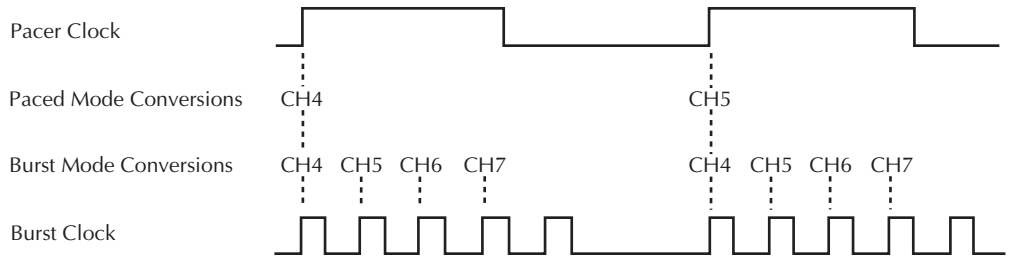
The paced mode, which is the default data-conversion mode, is the best mode for continuous, constant-rate scanning of each channel in a queue of channels. In the paced mode, one channel in the channel-gain queue is sampled and converted each time the pacer clock emits a pulse. The entire channel-gain queue is scanned at a rate equal to the pacer clock rate divided by the number of channels in the queue. Therefore, the sample rate — the rate at which an individual channel in the queue is repetitively sampled — is also equal to the pacer clock rate, divided by the number of channels in the queue. See Figure 2-4. The internal pacer clock is programmable via DriverLINX.

Burst conversion mode

The burst conversion mode is the best mode to use if you need to complete scans of the entire channel-gain queue quickly — close to simultaneously — and initiate scans of the entire queue at a significantly lower rate. For example, you would use the burst mode if you wish to complete scans of the entire queue at 1000 conversions/sec but initiate scans of the entire queue only every second.

In the burst mode, each pulse from the pacer clock initiates a burst of pulses from the burst clock which are emitted at the burst clock rate. Each pulse from the burst clock causes one channel in the queue to be sampled and converted, and burst clock pulses continue until the entire queue is scanned. In summary, scans of the channel-gain queue are repetitively initiated at a rate equal to the pacer clock rate, and scans of the queue are completed at a rate equal to the burst clock rate. Therefore, the sample rate — the rate at which an individual channel in the queue is repetitively sampled — is also equal to the pacer clock rate. See Figure 2-4.

Figure 2-4
Paced mode and burst mode timing for a queue of channels 4 to 7



Clock sources

KPCI-3108 boards provide two conversion clocks: a pacer clock and a burst mode clock. The use of these clocks in the paced and burst conversion modes is described in "Data conversion modes" and summarized in Figure 2-4. The clock sources themselves are described in the following subsections.

Pacer clock sources

The following clock sources may be used for paced mode conversions on KPCI-3108 boards:

- **Software clock source**

  KPCI-3108 boards allow you to acquire single samples under program control. In other words, conversions are controlled through the Windows interface rather than by hardware signals. When using a software conversion clock, the host computer issues a command to initiate a conversion. The host polls the board to determine if the conversion is complete. When the conversion is complete, the host reads the data from the A/D converter and returns the value.

  Software-initiated conversions are suitable for measuring DC voltages. However, in applications where you must accurately control the sampling rate (as when measuring time-varying signals), using either an internal or external hardware clock source is recommended, as described below.

- **Hardware clock source, internal (Internal pacer clock source)**

  The internal, onboard pacer clock source creates a pacer-clock timing signal using one or more 82C54 counter/timers and a crystal-controlled time base. (Refer to "Counter/timer features," near the end of Section 2, for an illustration.) The time base runs at 10MHz and provides divided frequencies of 5 MHz, 1 MHz, and 100 kHz. You can program the internal pacer clock rate via DriverLINX.

  You can use the internal pacer clock source to pace events other than analog-to-digital conversions (digital-to-analog conversions, for example). However, all events timed by the internal pacer clock source are paced at the same rate.

- **Hardware clock source, external (External pacer clock source)**

  An external pacer clock source is an externally applied TTL-compatible signal attached to bit IP0— pin 21 of the upper, "Analog" I/O connector, J1. Bit IP0 is a multi-function digital input; therefore you must use software to configure it as the external pacer clock (XPCLK) input. Also use software to select the active edge of the signal to be recognized as a clock pulse — either a positive, rising edge or a negative, falling edge.

  By using an external pacer clock source, you can sample at rates unavailable through the 82C54 counter/timer, at uneven intervals, or in response to external events. An external pacer clock source also allows you to synchronize multiple boards via a common timing signal.

  You can use the external pacer clock source in the paced conversion mode to pace individual analog-to-digital and/or digital-to-analog conversions. You can use the external pacer clock source in the burst conversion mode to pace space bursts of conversions. Refer to Figure 2-4.

NOTE *The A/D converter converts samples at a maximum of 100 ksamples/s (one sample every 10.0µs), and the practical throughput is lower in some applications. (Refer to the previous section entitled "Throughput"). If you use an external clock, ensure that it does not initiate conversions more frequently than the maximum throughput for your data acquisition setup.*

NOTE *Keep in mind that the maximum sample rate for an individual channel equals the maximum throughput divided by the number of channels in the channel-gain queue.*

NOTE *You cannot simultaneously use an external pacer clock source and the internal pacer clock source. However, you can simultaneously use a software trigger source to start analog input conversions while simultaneously using either an internal or external pacer clock source for other I/O operations.*

Burst clock source

In the burst mode, the burst clock sets the rate at which burst pulses are emitted and individual channels in the channel-gain queue are converted. The burst clock works with the pacer clock, which sets the rate at which groups of burst pulses are initiated. See Figure 2-4.

Burst clock and pacer clock frequencies are programmable, as follows:

- The burst clock rate can be set via DriverLINX. The maximum acceptable burst mode conversion clock rate is gain-sensitive, as explained in "Throughput."
- The pacer clock rate should be set no higher than the burst clock rate divided by the number of channels in the channel-gain queue.

Triggers

Triggers are external digital signals or, in some cases, threshold crossings of analog signals. Triggers act at a single instant in time, in contrast to gates, which start analog input operations when the gate is turned on and stop the input operations when the gate is turned off. (Refer also to "Gates" in this section.)

Trigger sources

Trigger sources may be internal or external, as follows:

- **Internal triggers**

  An internal trigger is a software command that starts or stops data acquisition.
- **External digital triggers**

  An external digital trigger is the rising or falling edge of a TTL-compatible signal that is connected to bit IP1—pin 3 of the upper, "Analog" I/O connector. Bit IP1 is a multi-function digital input; therefore you must use software to configure it as the trigger-in (TGIN) input. Also use software to program whether analog input operations start on either positive or negative triggering, which are defined as follows:
  - *Positive-edge triggering* — Triggering occurs on the rising edge of the trigger signal.
  - *Negative-edge trigger*ing — Triggering occurs on the falling edge of the trigger signal.

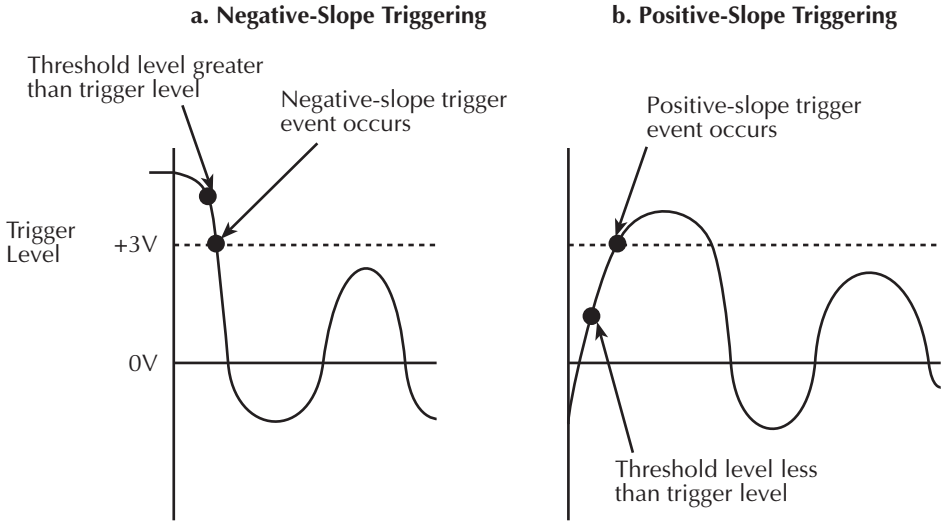
- **Analog triggers**

  An analog trigger is an event that occurs at a rising or falling voltage level on an analog input signal. Two software-selectable voltages specify where the analog trigger occurs: the trigger level and the threshold level. As shown in Figure 2-5 , if the threshold level is greater than the trigger level, triggering occurs on a negative slope. If the threshold level is less than the trigger level, triggering occurs on a positive slope.

  In the KPCI-3108, an analog trigger works specifically in the about-trigger acquisition mode. The acquisition is started by another internal or external trigger and continues after the analog trigger event until a specified number of samples has been acquired. For more information concerning about-trigger acquisition, refer to "Trigger acquisition modes" later in Section 2.

  Refer to your DriverLINX documentation for information about programming and configuring analog triggers.

Figure 2-5
Examples of analog trigger conditions



Trigger operation and clock source effects

The actual point at which conversions begin depends on whether the clock source is internal or external, as follows:

- **Internal trigger operation with internal clock source**

  If conversions are triggered with an internal trigger and timed via an internal pacer clock source, then conversions begin virtually immediately after the trigger, as follows:

  1. The 82C54 counter/timer is idle until the internal trigger occurs; after the trigger occurs, the first conversion begins virtually immediately.
  2. Subsequent conversions are synchronized to the internal clock.

  See Figure 2-6.

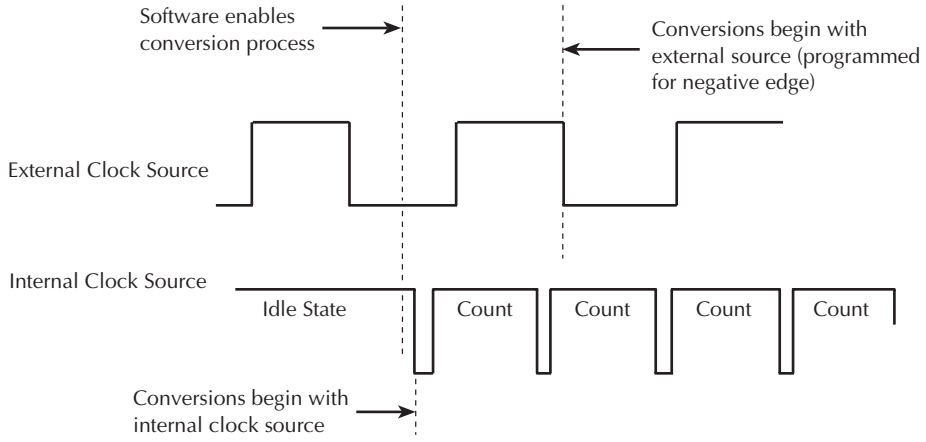
- **Internal trigger operation with external clock source**

  If conversions are triggered with an internal trigger and timed via an external clock source, then analog input operations are triggered as follows:

  1. Conversions are armed when the trigger occurs.
  2. Conversions begin with the next active edge of the external clock source.
  3. Conversions continue with subsequent active edges of the external clock source.

See Figure 2-6.

Figure 2-6
Enabling conversions with software triggers



- **External trigger operation with internal clock source**

  If conversions are triggered with an external trigger and timed via an internal pacer clock source, then analog input operations are triggered as follows:

  1. Conversions begin virtually immediately after the internal trigger:
  2. The 82C54 counter/timer is idle until the internal trigger occurs. However, after the trigger occurs, the first conversion begins within 400ns.
  3. Subsequent conversions are synchronized to the internal clock.

  See Figure 2-7.

- **External trigger operation with external clock source**

  If conversions are triggered with an external trigger and timed via an external clock source, then analog input operations are triggered as follows:

  1. Conversions are armed when the trigger occurs.
  2. Conversions begin with the next active edge of the external clock source.
  3. Conversions continue with subsequent active edges of the conversion clock.

  See Figure 2-7.

Figure 2-7
Enabling conversions with hardware triggers

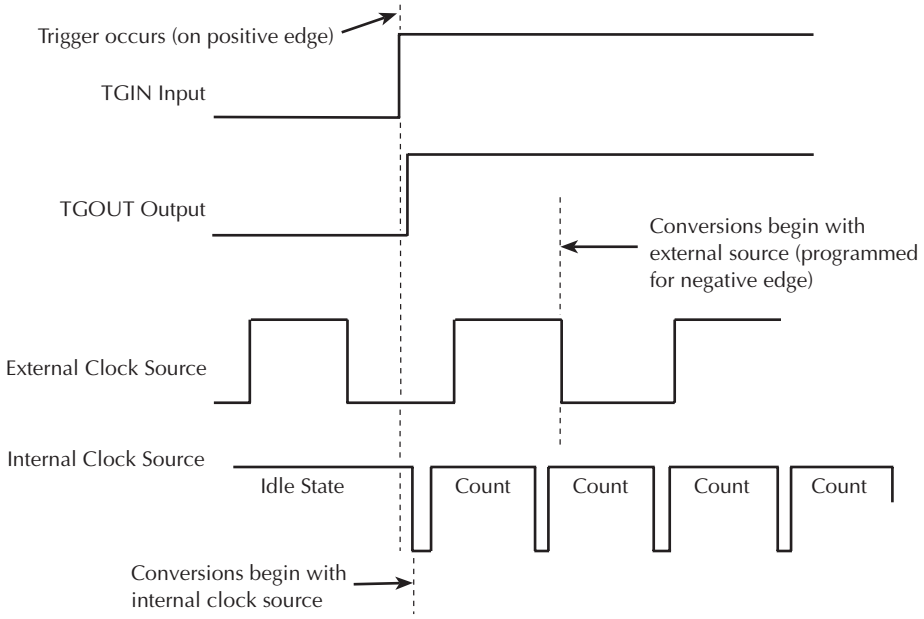


Figure 2-7 also shows that a pulse is initiated at the trigger out (TGOUT) digital output just following the external trigger pulse at the TGIN trigger input (the IP1 multi-function input configured as TGIN). For more information about TGOUT, refer to the section "The trigger-out (TGOUT) digital output function."

Trigger acquisition modes

Depending on your application, you may wish to use a trigger event to do one of the following: to start data collection, to halt data collection after a specified amount of additional data is collected, or to halt data collection abruptly. Three trigger modes are available in the KPCI-3108 to accomplish these objectives.

- **Post-trigger acquisition mode**

  In post-trigger acquisition, the data to be acquired appears after the trigger event. Post-trigger acquisition, starts after an internal or external trigger event and continues until a specified number of samples has been acquired or until the operation is stopped by software. See Figure 2-8a. Post-trigger, the most common trigger acquisition mode, has many obvious applications.

- **About-trigger acquisition mode**

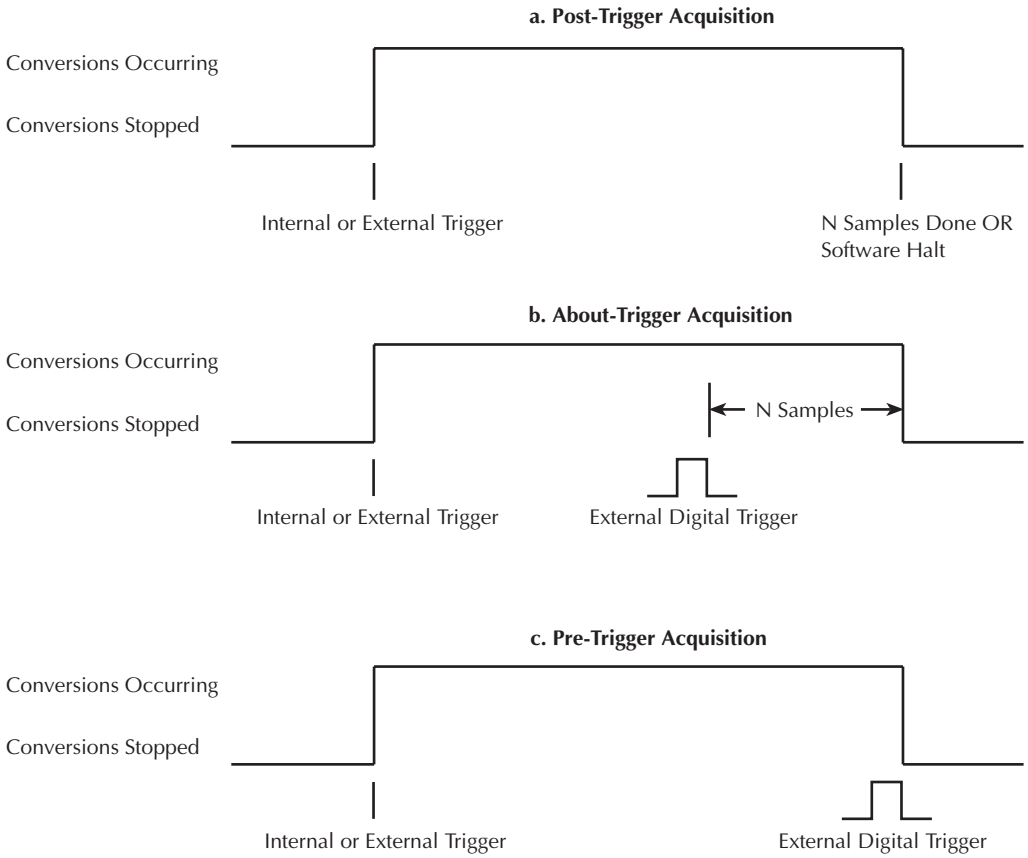
  In about-trigger acquisition, the data to be acquired appears before and after the trigger event. About-trigger acquisition is started by an internal or external trigger and continues after an external trigger event until a specified number of samples has been acquired. See Figure 2-8b. For example, if you were performing a car crash safety test, you might wish to do the following:

  1. Monitor speed and acceleration up to the point of impact.
  2. Emit an accelerometer-based trigger pulse at impact.
  3. Monitor crash-dummy impact forces and movement for a fixed number of samples after impact.

- **Pre-trigger acquisition mode**

  In the pre-trigger acquisition mode, the data to be acquired appears before the trigger event. A pre-trigger acquisition is started by an internal or external trigger and continues until an external trigger event occurs. See Figure 2-8c. For example, if you were monitoring an experimental process, you might wish to trigger process data acquisition to stop automatically at completion of the process.

Figure 2-8
Trigger acquisition modes



Gates

A gate is a digital input that allows conversions to proceed as long as the gate signal is active (logic high) and causes conversions to be halted as long as the gate signal is inactive (logic low). In other words, conversions can be started and stopped at will by turning the gate input on and off. (By contrast, a trigger acts at a single instant in time. Refer also to "Triggers" in this section.)

The gate input signal is a logic-high or logic-low TTL-compatible signal that is connected to bit IP1—pin 3 of the upper, "Analog" I/O connector. Bit IP1 is a multi-function digital input bit. Therefore you must software-configure it for gate input. This same input bit is used as the external trigger-in (TGIN) bit. However, it must be configured differently for the board to recognize incoming signals as gate signals instead of as trigger signals.

The way conversions are synchronized with a gate signal depends on whether you are using an internal clock or external clock source, as follows:

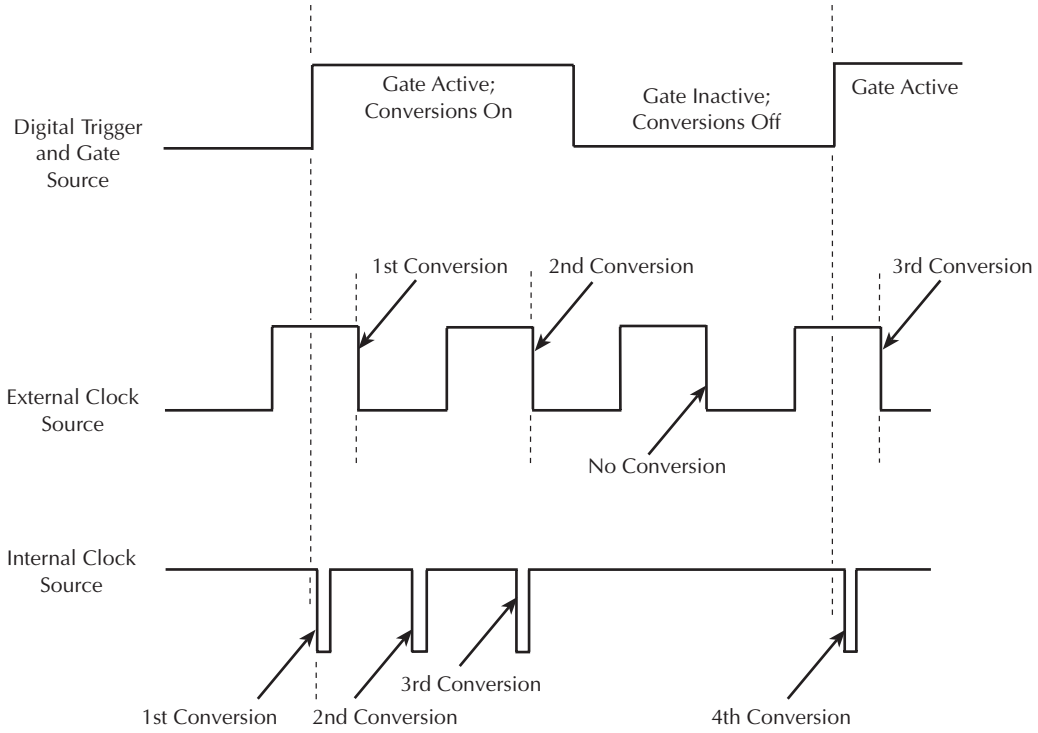
- **Gate operation with internal clock source**

  When using the gate input with an internal clock, conversions are synchronized with the internal gate signal. When the gate signal becomes active, the 82C54 counter is loaded (or reloaded) with an initial count value and starts counting, and data conversion starts (or resumes). When the gate signal becomes inactive, the 82C54 counter stops and data conversion stops. See Figure 2-9.

- **Gate operation with external clock source**

  When using the gate input with an external clock signal, conversions are synchronized with the external gate signal. When the gate signal becomes inactive, the signal from the external clock continues uninterrupted. See Figure 2-9.

Figure 2-9
Enabling conversions with gates



Analog output features

The analog output section of a KPCI-3108 board consists of two 16-bit DACs (digital-to-analog converters). Each DAC has four software-selectable ranges, as listed in Table 2-3.

Table 2-3
Analog output ranges and resolutions

Range	Resolution
±10.0 V	305 µV
±5.0 V	153 µV
0 to +10.0 V	153 µV
0 to +5.0 V	76 µV

The two DACs have output current ratings of ±5mA maximum and can drive capacitive loads of up to 100mF. The DAC output always initiates to 0V at power-up or reset.

The digital-to-analog conversion options resemble the analog-to-digital conversion options. The range and update sequence for one or both of the analog output channels is specified in a two-position, maximum, channel-gain queue. Both paced and burst conversion modes are available, as follows:

- In paced mode, one of the analog outputs specified in the channel gain queue is updated every time a pacer clock signal occurs. The pacer clock signal can be any of the following:
  - An internal hardware clock signal: an output pulse from an 82C54 counter/timer, the clock input of which is connected to a crystal-controlled time base.
  - An external hardware clock signal: the negative (falling) or positive (rising) edge of an external clock pulse.
  - A software update command: a write of an individual voltage value to a DAC by software. (This method is sometimes referred to as "level control.")
- In burst mode, both of the analog outputs specified in the channel-gain queue are sequentially updated every time that a hardware (only) pacer clock signal occurs. A burst clock determines the rate at which the updates occur. A typical user configures the burst clock rate to be much higher than the pacer clock rate. However, the burst clock rate must always be at least as large as the pacer clock rate times the number of positions (entries) in the channel gain queue. The maximum burst clock rate for digital-to-analog conversions is 500 kHz.

Refer also to the A/D paced and burst mode conversion discussions under "Data conversion modes" and "Clock sources" earlier in Section 2.

For information about wiring the analog outputs, refer to "Wiring analog output signals (KPCI-3108 board only)" in Section 3. For information about configuring and using the analog outputs, refer to your DriverLINX documentation and application software documentation.

Digital input and output features

This section discusses the following:

- The 32 general-purpose digital inputs and outputs
- The six multi-function digital inputs and six multi-function digital outputs, including:
  - Bit assignment options
  - Special functions

KPCI-3108 boards have 32 general-purpose digital inputs and outputs, six multi-function digital inputs, and six multi-function digital outputs. The general-purpose digital I/O and multi-function digital I/O are discussed in separate sections below

NOTE *For all digital I/O, logic 1 on an I/O line indicates that the input/output is high (greater than 2.0V); logic 0 on an I/O line indicates that the input/output is low (less than 0.8V). The digital inputs are compatible with TTL-level signals. Multi-function digital inputs are provided with 10kΩ pull-up resistors connected to +5V; therefore, multi-function digital inputs appear high (logic 1) if no signal is connected.*

General-purpose digital inputs and outputs

The lower, "Digital" I/0 connector provides 32 bits of high current I/O (15 mA max. source current at ≥2.0V, 64 mA max. sink output current at <0.55V). These general-purpose bits (the twelve multi-function digital I/O bits available at the upper "Analog" I/O connector may also be configured as general-purpose bits) are software-configurable as either inputs or outputs in groups of eight—each group of eight bits being handled by one of four eight-bit registers. These bits may be used for a variety of purposes, similarly to the bits of common digital I/O boards such as the PIO-24 and KPCI-PIO24. The output current capabilities of these bits are much higher than available from the industry-standard 8255 digital I/O chip.

Connector pin assignments for general-purpose digital I/O bits are summarized in Figure 3-3 of Section 3. Wiring of the general-purpose digital I/O is discussed in Section 3, specifically under "Wiring digital input and output signals" and generally under "Installing and wiring to the KPCI-3108 board." The electrical characteristics of the general purpose digital I/O are listed in Appendix A. Programming/configuring and using the general-purpose digital I/O is discussed in your DriverLINX documentation and/or your application software documentation.

Multi-function digital inputs and outputs

The upper "Analog" I/O connector provides twelve multi-function TTL I/O bits. Six of the bits, IP0 through IP5, are fixed as inputs (CMOS, as well as TTL, compatible). The other six bits, OP0 through OP5, are fixed as outputs.

Each of the six multi-function input bits may be used as a general-purpose digital input bit, or as a counter/timer access or acquisition control bit. Refer to Table 2-4.

Table 2-4
Specific bit assignments and descriptions for multi-function digital inputs

Bit assignment	Description
IP0	May be used as the following: • XPCLK, external pacer clock input • General-purpose input bit, target mode
IP1	May be used as the following: • TGIN, external trigger or gate input • General-purpose input bit, target mode
IP2	May be used as the following: • Counter/timer C/T0 external clock input • General-purpose input bit, target mode
IP3	May be used as the following: • Counter/timer C/T1 external clock input • General-purpose input bit, target mode
IP4	May be used as the following: • Counter/timer C/T0 external gate input • General-purpose input bit, target mode
IP5	May be used as the following: • Counter/timer C/T1 external gate input • General-purpose input bit, target mode

When a multi-function digital input bit is configured as general-purpose input bits, data is transferred via a DriverLINX target-mode-read service request. However, a multi-function digital input bit that is being used as a counter/timer access bit or acquisition control bit may also be read via a target-mode-read, without interfering with the counter/timer access or acquisition control function.

The functions of the first five multi-function output bits (OP0 through OP4) are configured in fixed groups rather than individually. Refer to Table 2-5. There are three group configuration modes: mode 0, mode 1, and mode 2. In any given mode, the bit functions of OP0 through OP4 are fixed; bit functions from the other two modes cannot be interlaced or overlapped.

- Mode 0 is the general-purpose output mode. In mode 0, outputs OP0 through OP4 can be used as target-mode digital outputs. The bits are set and cleared via a DriverLINX service request.
- Mode 1 is the counter/timer and acquisition-control output mode. In mode 1, outputs OP0 through OP4 provide access to all three counter/timer outputs and to two key acquisition-control outputs.
- Mode 2 is the multiplexer control mode. In mode 2, outputs OP0 through OP4 control address and gain selection of external multiplexers, as used in channel-expansion accessories such as the EXP-1800 and MB-02.

However, the sixth multi-function output bit (OP5) is configured individually—independently of mode 0, mode 1, and mode 2—for any of a variety of special functions. This bit gives you access to TGOUT, an output that tracks the pacer-clock, or the output of one counter/timer, even when controlling external multiplexers. Refer to Table 2-5.

Table 2-5
Specific bit assignments and descriptions for multi-function digital outputs

Output mode	Bit assign-ment	Description
0	OP0	General-purpose output bit, target-mode
	OP1	General-purpose output bit, target-mode
	OP2	General-purpose output bit, target-mode
	OP3	General-purpose output bit, target-mode
	OP4	General-purpose output bit, target-mode
	OP5	Configurable as one of the following: • TGOUT (trigger-out output) • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output
1	OP0	Frame sync
	OP1	Counter/timer C/T0 output
	OP2	Counter/timer C/T1 output
	OP3	Counter/timer C/T2 output
	OP4	Pacer-clock output
	OP5	Configurable as one of the following: • TGOUT (trigger-out) output • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output
2	OP0	External address bit 0 for multiplexing of expansion-accessory channels
	OP1	External address bit 1 for multiplexing of expansion-accessory channels
	OP2	External address bit 2 for multiplexing of expansion-accessory channels
	OP3	External address bit 3 for multiplexing of expansion-accessory channels
	OP4	External gain bit for some expansion accessories (e.g. EXP-1800)
	OP5	Configurable as one of the following: • TGOUT (trigger-out output) • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output

Connector pin assignments for the multi-function digital I/O bits are summarized in Figure 3-2. Wiring to the multi-function digital I/O is discussed in Section 3 under "Wiring digital input and output signals." Electrical characteristics of the multi-function digital I/O are listed in Appendix A. Configuring/programming and using the multi-function digital I/O is discussed in your DriverLINX documentation and/or your application software documentation.

Software-configurable special functions for the multi-function digital I/O are discussed briefly in the subsections that follow.

The external pacer clock (XPCLK) digital input function

You can configure multi-function bit IP0 as an external pacer-clock input (XPCLK). Then you can connect this input to an external hardware-clock source to time analog data conversions.

You cannot use the external pacer-clock source and the internal pacer-clock source simultaneously. However, you can simultaneously use the software-clock source to start analog data conversions while simultaneously using either an internal or external hardware-clock source.

For more information about the use of an external pacer clock, refer to the following headings earlier in Section 2: "Data conversion modes," "Clock sources," and "Analog output features."

The trigger in (TGIN) digital input function

You can configure multi-function bit IP1as an external digital trigger input (TGIN) or gate input. Then you can connect this input to an external TTL-compatible trigger or gate signal for starting and/or stopping analog-to-digital conversions.

For more information about the use of an external trigger signal, refer to "Triggers" and "Gates" earlier in Section 2.

The counter/timer clock digital input functions

Your board includes an 82C54 circuit that provides three counter/timers. You can configure the following multi-function digital I/O bits on the upper "Analog" I/O connector as external counter/timer clock inputs for two of the three 82C54 counter/timers:

- Bit IP2 is the external clock input for counter/timer C/T0.
- Bit IP3 is the external clock input for counter/timer C/T1.

There is no external counter/timer clock input for counter/timer C/T2

You can connect these inputs to external event or time base signals to perform a variety of tasks. For more information about the use of the 82C54 counter/timers, refer to "Counter/timer features" later in Section 2.

The counter/timer gate digital input functions

Your board includes an 82C54 circuit that provides three counter/timers. You can configure the following multi-function digital I/O bits on the upper "Analog" I/O connector as external counter/timer gate inputs for two of the three 82C54 counter/timers.

- Bit IP4 is the external gate input for counter/timer C/T0.
- Bit IP5 is the external gate input for counter/timer C/T1.

There is no external counter/timer gate input for counter/timer C/T2

You can connect the C/T0 and C/T1 gate inputs to external TTL signals to enable or disable C/T0 and C/T1.

For more information about the use of the 82C54 counter/timers, refer to "Counter/timer features" later in Section 2.

The trigger-out (TGOUT) digital output function

You can configure bit OP5 as a trigger-out (TGOUT) digital output, which is synchronized with internal and external trigger and gate signals.

If you use only the internal pacer clock to trigger analog I/O operations, you can use the TGOUT signal to synchronize analog I/O operations at multiple KPCI-3108 boards. Alternatively, you can use the TGOUT signal to trigger or gate user-specific events. The TGOUT signal has the following properties:

- **TGOUT signal with an external trigger input signal**

  When you start an analog input operation with an external trigger signal (at bit IP1 configured as the TGIN input), there is a delay of about 200ns between the active edge of the TGIN signal and the positive, rising edge of the TGOUT signal. See Figure 2-10a.

NOTE *TGOUT cannot be used with about-trigger acquisitions.*

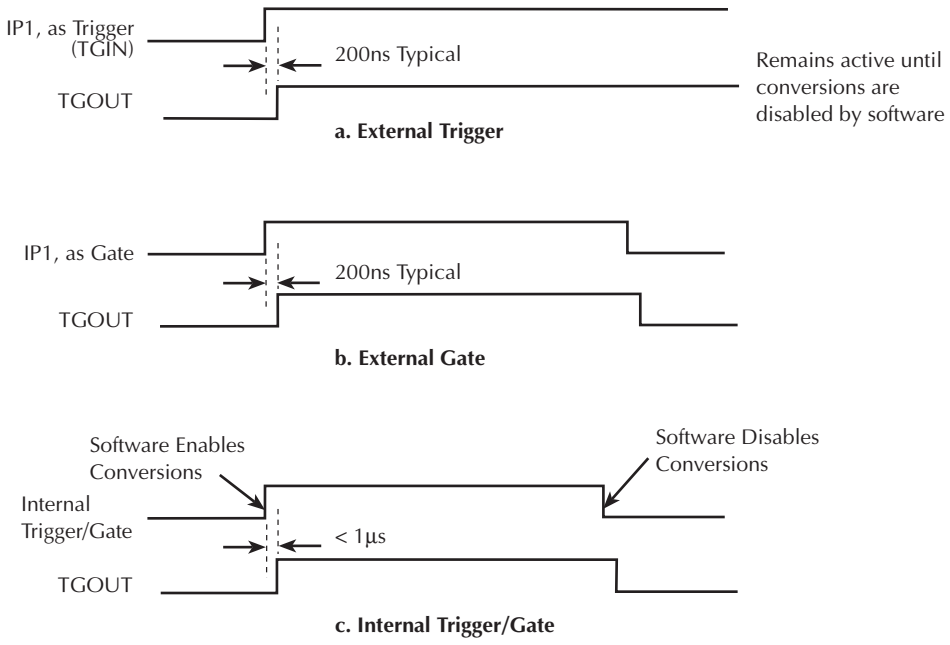
- **TGOUT signal with an external gate input signal**

  When you start an analog input operation via an external gate signal (at bit IP1 configured as a gate input), there is a delay of about 200ns between the active edge at IP1 and the positive, rising edge of TGOUT. See Figure 2-10b.
- **TGOUT signal with an internal trigger or gate signal**

  When you start an analog input operation via an internal trigger/gate, there is a delay of less than 1µs between the active edge of the internal trigger/gate and the positive, rising edge of TGOUT. See Figure 2-10c.

You may configure bit OP5 for TGOUT individually, independently of the three output options that configure the other five multi-function digital output bits (OP0 through OP4). Refer to Table 2-7.

Figure 2-10
Timing for the generation of TGOUT



The pacer-clock output function

The KPCI-3108 boards provides a pacer-clock output that is synchronized with the internal or external pacer clock, whichever is being used for A/D and/or D/A conversions. The external pacer-clock output may be used to synchronize A/D and/or D/A conversions with the operation of external devices connected to the board I/O connectors.

Under multi-function digital output option 0, configure bit OP4 as a pacer-clock output bit. You may also individually configure bit OP5 as a pacer-clock output bit, independently of the three output options that configure the other five multi-function digital output bits (OP0 through OP4). Refer to Table 2-5.

Frame sync digital output signal

Frame sync is a digital output signal that goes low (logic 0) just after completion of a scan of the channel-gain queue. This may be useful in the future for track and hold applications.

The counter/timer digital output functions

Your board includes an 82C54 circuit that provides three counter/timers. You can configure the multi-function digital output bits on the upper "Analog" I/O connector as external counter/timer clock outputs for all three 82C54 counter/timers, as follows:

- Bit OP1 is the external output for counter/timer C/T0.
- Bit OP2 is the external output for counter/timer C/T1.
- Bit OP3 is the external output for counter/timer C/T2.

You can connect these outputs to perform a variety of tasks.

For more information about the use of the 82C54 counter/timers, refer to "Counter/timer features" later in Section 2.

All three counter/timer outputs are simultaneously available when the board is configured for multi-function digital output option 0. Additionally, you may individually configure bit OP5 as the output for any of the counter/timers, independently of the three output options that configure the other five multi-function digital output bits (OP0 through OP4). Refer to Table 2-5.

The expansion-channel digital output functions

When you connect EXP-1800 expansion accessories or MB-02 signal conditioning /expansion accessories to your KPCI-3108 board, you must configure multi-function output bits as addresses to sequence the expanded I/O channels. You configure bits OP0, OP1, OP2, and OP3 as expansion channel addresses when you select output option 1.You simultaneously configure OP4 as an expansion accessory gain bit (required by some expansion accessories) when you select output option 1.

Table 2-5 summarizes the bit assignments under multi-function digital output option 1.

Counter/timer features

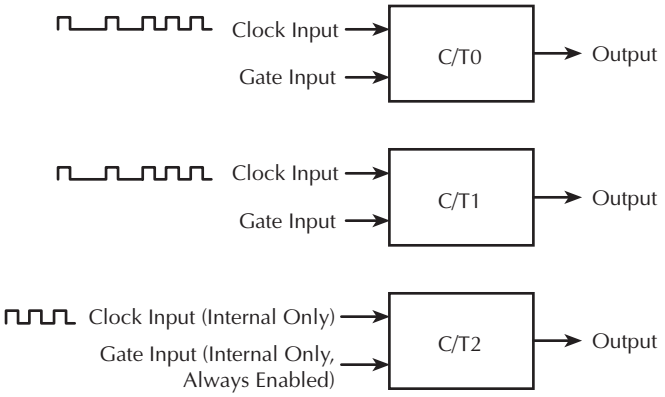
Each KPCI-3108 board includes an 82C54 circuit that contains three counter/timers: C/T0, C/T1, and C/T2. This section briefly discusses:

- The purpose and use of the counter/timers in general
- The counter/timer operational modes available with the KPCI-3108 board

Counter/timer general discussion

Each of the three counter/timers may be used to count event pulses or timing pulses, such as pulses from a precision time base. When the number of pulses it counts at its clock input equals a preset number—set via software—the counter/timer emits an output signal that may be used for a variety of purposes. For example, the output may be used as an event trigger, as a divided-frequency timing signal, or as the clock input for a second, cascaded counter/timer. Counting is either enabled continuously or is enabled or disabled through a gate input. Figure 2-11 illustrates the inputs and outputs of the three 82C54 counter/timers as implemented with the KPCI-3108 board.

Figure 2-11
Counter/timer I/O available on KPCI-3108 boards



The following summarizes the basic functions of the counter/timer inputs and outputs:

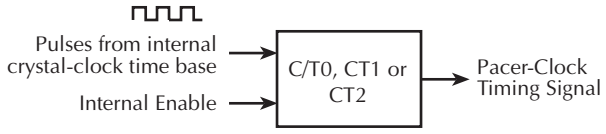
- The Clock input receives the event or time-base pulses that are counted.
- The Gate input receives a signal that enables or disables the counting process.
- The Output signals that the specified count has been achieved.

C/T2 accepts only internal clock signals and is enabled only internally and continuously. However, C/T2 may be used to extend the range of CT/0 or CT/1 by cascading—counting output pulses from CT/0 or CT/1.

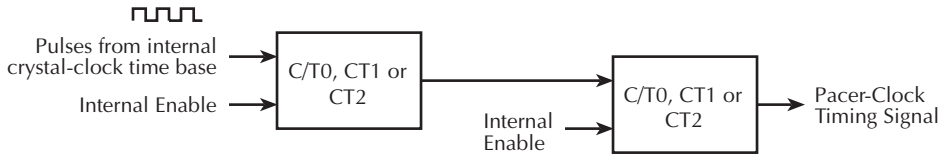
A key application that illustrates use of the counter/timers is pacer-clock timing. When scanning input channels, your board can use pacer-clock timing signals to regularly space individual analog-to-digital and/or digital-to-analog conversions or bursts of conversions. (Refer to "Data conversion modes," "Clock sources," and "Analog output features" earlier in Section 2.) Any of the three counter/timers may be used for pacer-clock timing. Note, however, that 82C54 timer/counters are not required for the *burst*-clock, which is generated by a different route. Production of internally-generated pacer-clock timing pulses is illustrated in Figure 2-12.

Figure 2-12
Using counter/timers for internal pacer-clock

a. Using one counter/timer for pacer-clock timing



b. Using two counter/timers, cascaded, for pacer-clock timing



In this application, each counter acts as a frequency divider. For example, if in Figure 2-12a the crystal-clock time base is configured for 1 MHz (10, 5, 1, and 0.1 MHz are available) and the counter/timer is set for 100 counts, a pacer-clock timing pulse is emitted only once per 100 time-base pulses. Therefore, the time-base frequency is divided by 100, and the output frequency is 10 KHz. If in Figure 2-12b the crystal-clock time base is configured for 1 MHz, and both counter/timers are set for 100 counts, the time-base frequency is divided by a factor of (100 x 100), and the output frequency is 100 Hz.

Four of the multi-function digital input bits at the upper "Analog" I/O connector are independently software-configurable as counter/timer inputs for C/T0 and C/T1, as follows:

- The external clock input for counter/timer C/T0 is bit IP2 (pin 20).
- The external clock input for counter/timer C/T1 is bit IP3 (pin 2).
- The external gate input for counter/timer C/T0 is bit IP4 (pin 19).
- The external gate input for counter/timer C/T1 is bit IP5 (pin 1).

You can attach a 0 MHz to100 kHz external clock source to the clock inputs. Pull-up resistors of 10 kΩ are provided at the gate input pins; therefore, the gates appear enabled if no signal is attached to the gate inputs.

The following three multi-function digital output bits are configured as counter/timer outputs — together as a group — under output option 0:

- The output bit for counter/timer C/T0 is OP1 (pin 6 at the upper "Analog" I/O connector).
- The output bit for counter/timer C/T1 is OP2 (pin 23 at the upper "Analog" I/O connector).
- The output bit for counter/timer C/T2 is OP3 (pin 5 at the upper "Analog" I/O connector).

Additionally, multi-function digital output bit OP5 is independently configurable as C/T0, C/T1, or C/T2 (at pin 4 at the upper "Analog" I/O connector).

For more information about multi-function digital output options, refer to the section above, "Multi-function digital inputs and outputs." Refer also to "Wiring counter/timer signals" in Section 3.

Counter/timer operational modes

The 82C54 counter/timer circuit provides software-configurable operational modes to perform various functions. The following modes are available from the 82C54 counter/timer. All may not be available for use with the KPCI-3108 board. Refer to your DriverLINX documentation to determine which modes are available.

- Pulse on terminal count (Mode 0)
- Programmable one-shot (Mode 1)
- Rate generator (Mode 2)
- Square-wave generator (Mode 3)
- Software-triggered strobe (Mode 4)
- Hardware-triggered strobe (Mode 5)

Each of these modes is explained briefly in the subsections that follow. Refer to the DriverLINX *Counter/Timer Programming Guide* for more details.

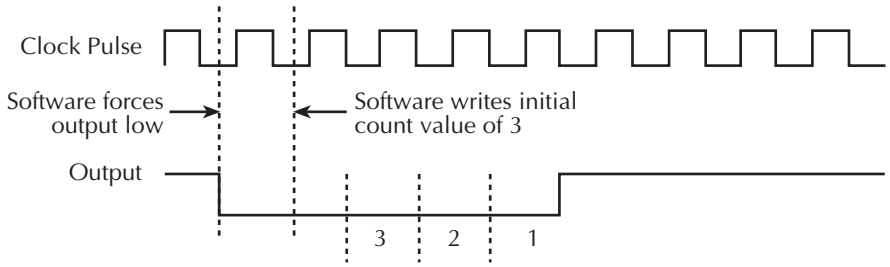
Pulse on terminal count (counter/timer mode 0)

The pulse-on-terminal-count mode is useful for event counting or for programming a time delay. Software is used to force the output low. On the next clock pulse after the software writes the initial count value, the counter is loaded. When the counter reaches zero, the output goes high and remains high until the software writes a new count value. Note that the output does not go high until $n + 1$ clock pulses after the initial count is written, where n indicates the loaded count.

A high gate input enables counting; a low gate input disables counting. The gate input has no effect on the output. Note that an initial count value written while the gate input is low is still loaded on the next clock pulse.

Figure 2-13 illustrates pulse-on-terminal-count mode.

Figure 2-13
Pulse-on-terminal-count counter/timer mode



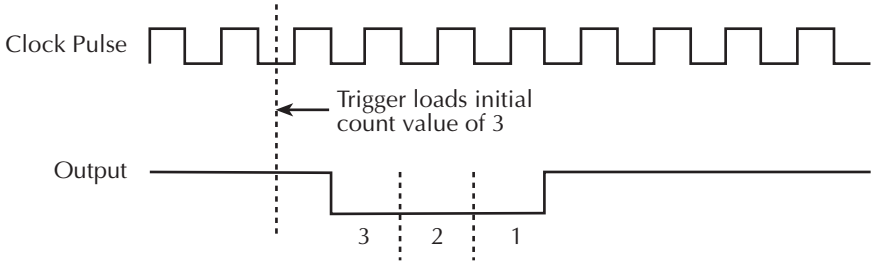
Programmable one-shot (counter/timer mode 1)

The programmable one-shot mode is useful for providing a hardware-triggered delay or one-shot pulse. The output is initially high. A trigger loads the initial count value into the counter. At the next clock pulse after the trigger, the output goes low and remains low until the counter reaches zero. (The one-shot pulse is *n* clock cycles in duration, where *n* indicates the loaded count.) After the counter reaches zero, the output goes high and remains high until the clock pulse after the next trigger; this makes the one-shot pulse retriggerable.

You do not have to reload the count into the counter. The gate input has no effect on the output. Writing a new count to the counter during a one-shot pulse does not affect the current one-shot pulse.

Figure 2-14 illustrates programmable one-shot mode.

Figure 2-14
Programmable one-shot counter/timer mode



Rate generator (counter/timer mode 2)

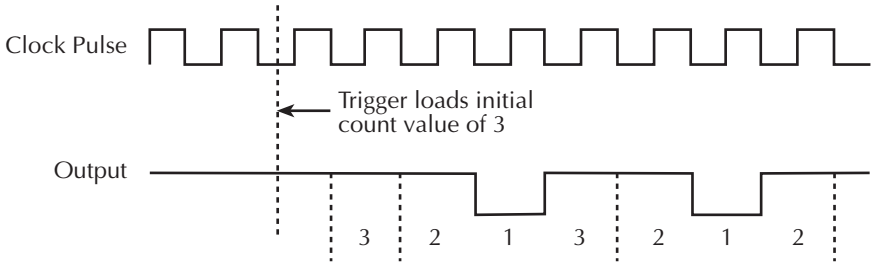
The rate-generator mode is useful for generating a real-time clock interrupt. The output is initially high. A trigger loads the initial count value into the counter. At the next clock pulse after the trigger, the counter starts counting down. When the counter reaches one, the output goes low for one clock pulse and then goes high again. The counter is then reloaded with the initial count value and the process repeats.

A high gate input enables counting; a low gate input disables counting. If the gate goes low during an output pulse, the output is set high immediately; this allows you to use the gate input to synchronize the counter.

Writing a new count to the counter while counting does not affect the current counting sequence. In this mode, a count of 1 is illegal.

Figure 2-15 illustrates rate generator mode.

Figure 2-15
Rate-generator counter/timer mode



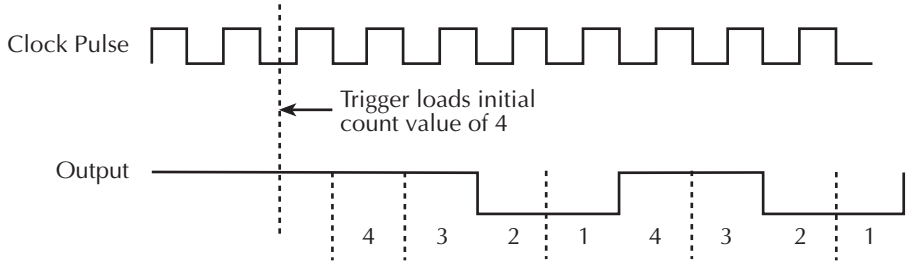
Square-wave generator (counter/timer mode 3)

This mode is useful for square-wave generation. The output is initially high. A trigger loads the initial count value into the counter. At the next clock pulse after the trigger, the counter starts counting down. When half the initial count has elapsed, the output goes low for the remainder of the count. When the total count elapses, the counter is reloaded with the initial count value, the output goes high again, and the process repeats. If the initial count is odd, the output is high for (n + 1) / 2 counts and low for (n - 1) / 2 counts, where n indicates the loaded count.

A high gate input enables counting; a low gate input disables counting. If the gate goes low while the output is low, the output is set high immediately; this allows you to use the gate input to synchronize the counter.

Figure 2-16 illustrates square-wave generator mode.

Figure 2-16
Square-wave generator counter/timer mode



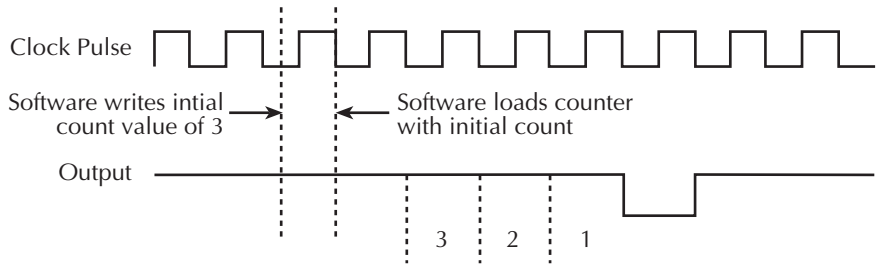
Software-triggered strobe (counter/timer mode 4)

When the counter/timer is in the software-triggered strobe mode, the output is initially high. Writing the initial count through software loads the initial count value into the counter at the next clock pulse, but the counter does not start counting. At the next clock pulse, the counter starts counting down. When the counter reaches zero, the output goes low for one clock pulse and then goes high again. Note that the output does not go low until n + 1 clock pulses after the initial count is written, where n indicates the loaded count.

A high gate input enables counting; a low gate input disables counting. The gate input has no effect on the output.

Figure 2-17 illustrates software-triggered strobe mode.

Figure 2-17
Software-triggered strobe counter/timer mode



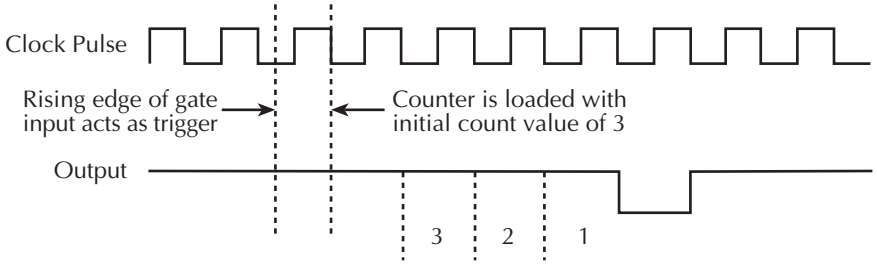
Hardware-triggered strobe (counter/timer mode 5)

When the counter/timer is in the software-triggered strobe mode, the output of the counter/timer is initially high. A rising edge of the gate input acts as a trigger. The counter is loaded with the initial count value on the next clock pulse after the trigger, but the counter does not start counting. At the next clock pulse, the counter starts counting down. When the counter reaches zero, the output goes low for one clock pulse and then goes high again. Note that the output does not go low until *n* + 1 clock pulses after the trigger event occurs, where *n* indicates the loaded count.

After the trigger event occurs, the gate input has no effect on the output. Writing a new value during counting does not affect the counting sequence.

Figure 2-18 illustrates hardware-triggered strobe mode.

Figure 2-18
Hardware-triggered strobe counter/timer mode



Power

A KPCI-3108 board requires +5V at 0.8A from the host computer power bus and +12V at 0.5A from this power bus to operate onboard circuits.

Additionally, +5V power for light duty external circuits—at a maximum **total** current draw of 1A— may be drawn indirectly from the host computer power bus via the board I/O connectors. The +5V is available at pin 25 of the upper "Analog" I/O connector and pins 35 and 36 of the lower "Digital" I/O connector.

CAUTION **Do not connect the +5V outputs to external power supplies. Connecting these outputs to external power supplies may damage the external supplies, the board, and the computer.**

Do not draw more than 1.0A, total, from all +5V outputs combined. Drawing more than 1.0A, total, may damage the board. Also keep in mind that the 5V output comes from the computer power bus. Know the limits of the computer 5V power bus and the current drawn from it by other boards and devices. Other demands on the 5V power bus may limit the current drawn from your board to less than 1.0A.

3
Installation

This section describes system installation, in the following order:

- Software options and installation guidelines. (Note: install the software before installing the hardware.)
- Hardware installation, including the following:
  - Unwrapping and inspecting the board
  - Physically installing the board
  - Checking the combined board and DriverLINX installation
  - Identifying the I/O connector pins
  - Wiring your circuits to the I/O connector pins (via the wiring accessories)
  - Synchronizing multiple boards
  - Powering your circuits from the board

Installing the software

NOTE *Install the DriverLINX software before installing the KPCI-3108 board. Otherwise, the device drivers will be more difficult to install.*

Software options

Users of KPCI-3108 boards have the following two software options. In both cases, the software interfaces with your system via the DriverLINX software provided with your board:

- The user can run a fully integrated data-acquisition software package such as TestPoint or LabVIEW.
- The user can write and run a custom program in Visual C/C++, Visual Basic, or Delphi, using the programming support provided in the DriverLINX software.

A summary of the pros and cons of using integrated packages or writing custom programs is provided in the Keithley Full Line Catalog.

The KPCI-3108 has fully functional driver support for use under Windows 95/98/NT.

DriverLINX driver software for Windows 95/98/NT

DriverLINX software, supplied by Keithley with the KPCI-3108 board, provides convenient interfaces to configure analog and digital I/O modes without register-level programming.

Most importantly, however, DriverLINX supports those programmers who wish to create custom applications using Visual C/C++, Visual Basic, or Delphi. DriverLINX accomplishes foreground and background tasks to perform data acquisition. The software includes memory and data buffer management, event triggering, extensive error checking, and context sensitive online help.

DriverLINX provides application developers a standardized interface to over 100 services for creating foreground and background tasks for the following:

- Analog input and output
- Digital input and output
- Time and frequency measurement
- Event counting
- Pulse output
- Period measurement

In addition to basic I/O support, DriverLINX also provides:

- Built-in capabilities to handle memory and data buffer management.
- A selection of starting and stopping trigger events, including pre-triggering, mid-point triggering and post-triggering protocols.
- Extensive error checking.
- Context-sensitive on-line help system DriverLINX is essentially hardware independent, because its portable APIs (Application Programming Interfaces) work across various operating systems. This capability eliminates unnecessary programming when changing operating system platforms.

TestPoint™

TestPoint is a fully featured, integrated application package that incorporates many commonly used math, analysis, report generation, and graphics functions. The TestPoint graphical drag-and-drop interface can be used to create data acquisition applications, without programming, for IEEE-488 instruments, data acquisition boards, and RS232-485 instruments and devices.

TestPoint includes features for controlling external devices, responding to events, processing data, creating report files, and exchanging information with other Windows programs. It provides libraries for controlling most popular GPIB instruments. OCX and ActiveX controls plug directly into TestPoint, allowing additional features from third party suppliers.

TestPoint interfaces with your KPCI-3108 board through DriverLINX, using a driver that is provided by the manufacturer.

LabVIEW™

LabVIEW is a fully featured graphical programming language used to create virtual instrumentation. It consists of an interactive user interface, complete with knobs, slide switches, graphs, strip charts, and other instrument panel controls. Its data-driven environment uses function blocks that are virtually wired together and pass data to each other. The function blocks, which are selected from palette menus, range from arithmetic functions to advanced acquisition, control, and analysis routines. Also included are debugging tools, help windows, execution highlighting, single stepping, probes, and breakpoints to trace and monitor the data flow execution. LabVIEW can be used to create professional applications with minimal programming.

A Keithley VI palette provides standard virtual instruments (VIs) for LabVIEW that interface with your KPCI-3108 board through DriverLINX. The needed driver is provided on your DriverLINX CD-ROM.

Installing DriverLINX

Refer to the instructions on the *Read this first* sheet and the manuals on the DriverLINX CD-ROM, both shipped with your board, for information on installing and using DriverLINX.

Installing application software and drivers

Installing the TestPoint software and driver

The DriverLINX driver for TestPoint is provided as part of the TestPoint software. The driver therefore installs automatically when you install TestPoint.

You can install TestPoint application software, made by Capital Equipment Corporation (CEC), at any time — before or after installing DriverLINX and the KPCI-3108 board. For TestPoint installation instructions, consult the manual provided by CEC.

NOTE *Before using TestPoint with the KPCI-3108 version of DriverLINX, check with CEC to ensure that your version of TestPoint is compatible with DriverLINX.*

Installing the LabVIEW software and driver

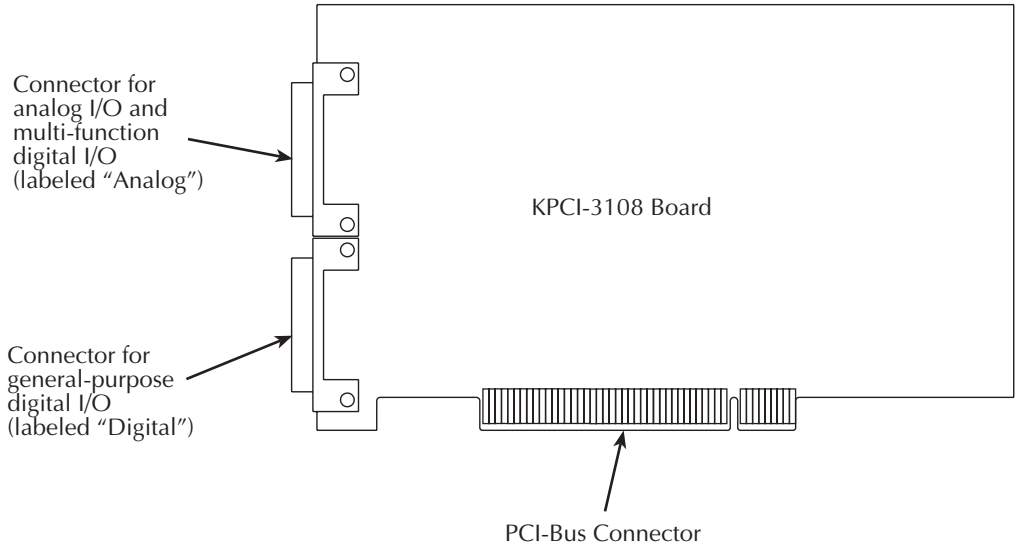
A DriverLINX driver for LabVIEW is provided on your DriverLINX CD-ROM. The LabVIEW driver does not install automatically when you install DriverLINX and your board. You must first install the LabVIEW application program, then install the DriverLINX driver. Access the LabVIEW driver installation routine by starting setup.exe on the DriverLINX CD-ROM, then selecting LabVIEW™ Support from the Install These DriverLINX components screen.

Consult the manual provided by National Instruments for LabVIEW installation instructions.

Installing and wiring to the KPCI-3108 board

The remainder of this section describes physically installing the KPCI-3108 board, connecting interfaces to the board, and wiring circuits to the interfaces. KPCI-3108 board connectors involved in these operations are labeled in Figure 3-1.

Figure 3-1
Connectors on the KPCI-3108 board


Connector for analog I/O and multi-function digital I/O (labeled "Analog")
KPCI-3108 Board
Connector for general-purpose digital I/O (labeled "Digital")
PCI-Bus Connector

The remainder of this section is ordered according to the following recommended installation sequence:

1. Install the board in your computer, as described in "Installing the board."
2. Check the installation as described in "Checking the combined board and DriverLINX installations."
3. Review the I/O connections for each pin on the two 36-pin I/O connectors of your board. Connector pin assignments for the KPCI-3108 boards are identified and described under "Identifying I/O connector pin assignments for KPCI-3108."
4. Connect the appropriate screw terminal and other interface accessory(s) to your board, using an appropriate cable assembly(s). One or more accessories are required to wire the board to your circuits. These accessories range from basic screw terminal connectors (STP-36 or STP-36/C) to signal conditioning and expansion accessories. Use of interface accessories and cables is described under "Connecting interface accessories to a KPCI-3108 board."
5. Wire your circuits to the interface accessories that you connected to the board in step 4. Refer to the sections "Wiring analog input signals," "Wiring analog output signals (KPCI-3108 board only)," "Wiring digital input and output signals," and "Wiring counter/timer signals."
6. If you wish to synchronize multiple KPCI-3108 boards, interconnect the trigger or gate signals as described under "Synchronizing multiple boards."
7. If you desire to use KPCI-3108 board power for any of your circuits, be sure to read "Wiring +5V power to external circuits" before proceeding.

Installing the board

CAUTION **Ensure that the computer is turned OFF before installing or removing a board. Installing or removing a board while power is ON can damage your computer, the board, or both.**

Handle the board in a static-controlled workstation; wear a grounded wrist strap. Discharge static voltage differences between the wrapped board and the handling environment before removing the board from its protective wrapper. Failure to discharge static electricity before and during handling may damage semiconductor circuits on the board.

Handle the board using the mounting bracket. Do not touch the circuit traces or connector contacts when handling the board.

Checking resources for the board

Ensure that your computer has sufficient resources, particularly power resources, to run your KPCI-3108 board. Check the capacity of the computer power supply and the power requirements of your computer and presently installed boards. Adding a KPCI-3108 board requires an additional 0.8A at +5V, maximum, and an additional 0.5A at +12V, maximum. If necessary, free resources by uninstalling other boards.

Unwrapping and inspecting the KPCI-3108 board

NOTE *Install the DriverLINX software before installing the KPCI-3108 board. Otherwise, the device drivers will be more difficult to install.*

After you remove the wrapped board from its outer shipping carton, unwrap and inspect it as follows:

1. Your board is packaged at the factory in an anti-static wrapper. Do not remove the anti-static wrapper until you have discharged any static electricity voltage differences between the wrapped board and the environment. Wear a grounded wrist strap. A grounded wrist strap discharges static electricity from the wrapped board as soon as you hold it. Keep the wrist strap on until you have finished installing the board.
2. Remove the KPCI-3108 board from its anti-static wrapping material. (You may wish to store the wrapping material for future use.)
3. Inspect the board for damage. If damage is apparent, arrange to return the board to the factory. Refer to Section 6, "Technical support."
4. Check the remaining contents of your package against the packing list and report any missing items immediately.
5. If the inspection is satisfactory, continue with "Installing the KPCI-3108 board."

Installing the KPCI-3108 board

WARNING **Be sure to reinstall the cover of your computer after installing the board.**

Install a KPCI-3108 board in a PCI expansion slot on your computer as follows:

1. Turn power OFF to the computer and to any external circuits attached to the board.

2. Remove the computer chassis cover.
3. Select an unoccupied PCI expansion slot in the rear panel, and remove the corresponding dummy mounting plate.
4. Insert the PCI connector of the board into the selected PCI slot of the computer. Take care not to interfere with neighboring boards. Ensure that the board is properly seated in the slot.
5. Secure the mounting bracket of the board to the chassis, using the retaining screw that you removed when you removed the dummy mounting plate.
6. Continue with "Configuring the board to work with DriverLINX."

Configuring the board to work with DriverLINX

After physically installing the board, do the following:

1. Turn on and reboot the computer. The DriverLINX Plug and Play Wizard screen appears.
2. Run the Wizard immediately by following the progressive instructions on the screen.
3. Continue with "Checking the combined board and DriverLINX installations."

If you do not run the Wizard immediately, it will not appear the next time you reboot. You must then start the Wizard from a batch file, as follows:

1. Open the Windows Explorer.
2. Double click on X:\DrvLINX4\Help\kpci3108.bat, where X = the letter of the drive on which you installed DriverLINX.

   The Wizard appears.

NOTE *You can also start this batch file directly from the CD-ROM by double clicking on Y:\DrvLINX4\Help\kpci3108.bat, where Y = the drive letter of your CD-ROM drive.*

3. Run the Wizard by following the progressive instructions on the screen.
4. Continue with "Checking the combined board and DriverLINX installations."

Checking the combined board and DriverLINX installations

Before making any connections to the board, check whether DriverLINX and your board are installed correctly and working together properly. Do this using the first two steps of "Problem isolation Scheme B: installation" in Section 6. The first two steps evaluate whether the DriverLINX Analog I/O Panel utility starts properly. If the Panel does not start properly at first, remaining steps lead you through diagnostic and remedial efforts. If necessary, steps lead you to deinstall, then reinstall DriverLINX and the board.

Do the following:

1. Turn ON your computer and boot Windows 95, 98, or NT.
2. Perform the first two steps of "Problem isolation Scheme B: installation" in Section 6.
3. If you cannot initially run the Analog I/O Panel, perform additional steps of "Problem isolation Scheme B: installation" as directed.
4. After DriverLINX and your board are installed properly and working together, continue with "Identifying I/O connector pin assignments for KPCI-3108," and then "Connecting interface accessories to a KPCI-3108 board."

Identifying I/O connector pin assignments for KPCI-3108

You connect a KPCI-3108 board to your signals via two IEEE 1284 36-pin mini-D connectors, located at the rear of the board.

- Figure 3-2 and Table 3-1 show and describe pin assignments and signal descriptions for the upper "Analog" I/O connector, through which analog I/O and multi-function digital I/O signals are connected. Identically numbered assignments and descriptions apply to the terminals on either of the following (described in the next section) if it is connected to the "Analog" I/O connector:
  - An STP-36 Series screw-terminal accessory (STP-36 or STP-36/C)
  - An STA-3108-A Series adapter/screw-terminal accessory (STA-3108-A1, STA-3108-A2, STA-3108-A3)

Figure 3-2
Pin assignments for KPCI-3108 upper "Analog" I/O connector pin

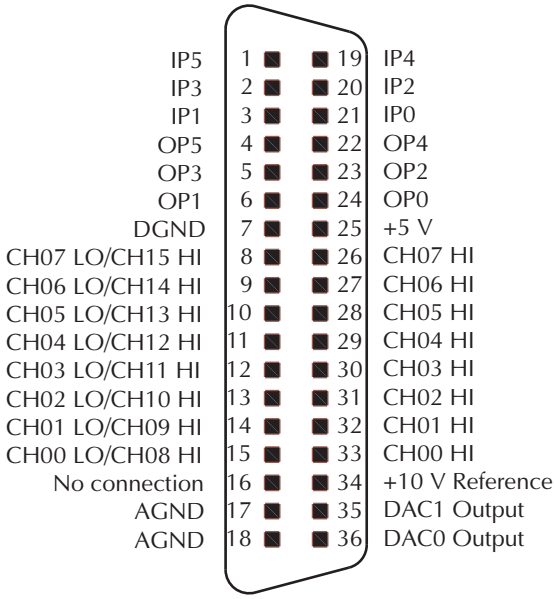

IP5 1 19 IP4
IP3 2 20 IP2
IP1 3 21 IP0
OP5 4 22 OP4
OP3 5 23 OP2
OP1 6 24 OP0
DGND 7 25 +5 V
CH07 LO/CH15 HI 8 26 CH07 HI
CH06 LO/CH14 HI 9 27 CH06 HI
CH05 LO/CH13 HI 10 28 CH05 HI
CH04 LO/CH12 HI 11 29 CH04 HI
CH03 LO/CH11 HI 12 30 CH03 HI
CH02 LO/CH10 HI 13 31 CH02 HI
CH01 LO/CH09 HI 14 32 CH01 HI
CH00 LO/CH08 HI 15 33 CH00 HI
No connection 16 34 +10 V Reference
AGND 17 35 DAC1 Output
AGND 18 36 DAC0 Output

Table 3-1
Signal descriptions for "Analog" I/O connector pins and screw-terminals

Pin or terminal	Assignment	Description	
1 2 3	IP5 IP3 IP1	Multi-function digital input bits, user-configurable for: • Counter/timer timebase and/or gate inputs • External pacer for A/D or D/A conversion • External digital trigger • Target-mode digital input	
4 5 6	OP5 OP3 OP1	Multi-function digital output bits, user-configurable for: • Counter/timer outputs • Trigger output • Control/addressing for expansion and signal conditioning accessories • Pacer clock output • Target-mode digital output	
7	DGND	Digital ground.	
   8 9 10 : 15	 CH07 LO/CH15 HI CH06 LO/CH14 HI CH05 LO/CH13 HI : CH00 LO/CH08 HI	Analog inputs, which function as follows for inputs configured as differential: • Channel 07 low-level input • Channel 06 low-level input • Channel 05 low-level input : • Channel 00 low-level input	Analog inputs, which function as follows for inputs configured as single-ended: • Channel 15 high-level input • Channel 14 high-level input • Channel 13 high-level input : • Channel 08 high-level input
16	No connection		
17, 18	AGND	Analog ground. (Refer to "Wiring analog input signals.")	
19 20 21	IP4 IP2 IP0	Multi-function digital input bits, user-configurable for: • Counter/timer timebase or gate inputs • External pacer for A/D or D/A conversion • External digital trigger • Target-mode digital input	
22 23 24	OP4 OP2 OP0	Multi-function digital output bits, user-configurable for: • Counter/timer outputs • Trigger output • Control/addressing for expansion and signal conditioning accessories • Pacer clock output • Target-mode digital output	
25	+5 V	+ 5 VDC from computer bus. (Refer to "Wiring +5V power to external circuits.")	
26 27 28 : 33	CH07 HI CH06 HI CH05 HI : CH00 HI	Channel 07 high-level input Channel 06 high-level input Channel 05 high-level input : Channel 00 high -level input	
34	+10 V Reference	Precision +10 VDC reference voltage source, which is designed to be connected to a high-impedance reference input only (supplied through a 1 KΩ series resistor).	
35	DAC1 Output*	Analog output from digital-to-analog converter number 1*	
36	DAC0 Output*	Analog output from digital-to-analog converter number 0*	

*This feature is not included with the KPCI-3107.

- Likewise, Figure 3-3 and Table 3-2 show and describe pin assignments and signal descriptions for the lower "Digital" I/O connector, through which 32 bits of general-purpose, high-current digital I/O are connected. Identically numbered assignments and descriptions apply to the terminals on either of the following (described in the next section) if it is connected to the "Digital" I/O connector:
  - An STP-36 Series screw-terminal accessory (STP-36 or STP-36/C)
  - An STA-3108-D1 Series adapter/screw-terminal accessory

Figure 3-3
Pin assignments for KPCI-3108 lower "Digital" I/O connector pins

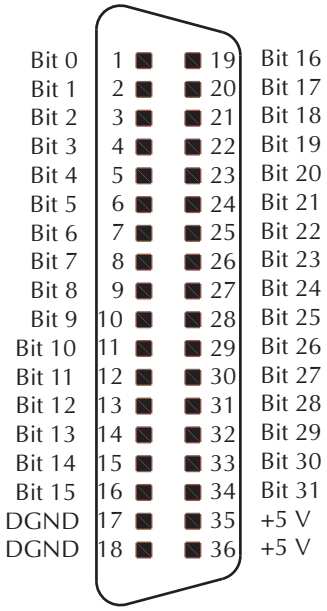


Table 3-2
Signal descriptions for "Digital" I/O connector pins and screw-terminals

"Digital" connector pin or STP-36 terminal	**Bit assignment**	**Description**
1 2 3 : 8	Bit 0 Bit 1 Bit 2 : Bit 7	General-purpose digital I/O bits, channel 0. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
9 10 11 : 16	Bit 8 Bit 9 Bit 10 : Bit 15	General-purpose digital I/O bits, channel 1. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
17, 18	DGND	Digital grounds. (Refer to "Wiring general-purpose digital I/O signals.")
19 20 21 : 26	Bit 16 Bit 17 Bit 18 : Bit 23	General-purpose digital I/O bits, channel 2. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
27 28 29 : 34	Bit 24 Bit 25 Bit 26 : Bit 31	General-purpose digital I/O bits, channel 3. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
35, 36	+5V	+ 5 VDC from computer bus. (Refer to "Wiring +5V power to external circuits.")

Connecting interface accessories to a KPCI-3108 board

CAUTION **The two I/O connectors of KPCI-3108 board, labeled "Analog" and "Digital," are mechanically identical. Ensure that you connect interface accessories and, indirectly, external circuits to the correct I/O connector. Connecting interface accessories or external circuits to the wrong connector may result in damage to the KPCI-3108 board, the host computer, your external circuits, or all three.**

Use combinations of the following interface accessories to wire your circuits to the KPCI-3108 I/O connectors

- Basic screw-terminal accessories
- Channel-expansion, signal-conditioning, or digital I/O accessories, combined with adapter/screw-terminal accessories
- Interconnection cables

Section 1 summarized the available interface accessories in Table 1-2, Table 1-3, and Table 1-4. This section describes how to interconnect these accessories, as follows:

- The first subsection describes the STP-36 (or STC-36/C) screw-terminal accessory and how to connect it to your board.
- The second subsection through the fifth subsection describe various channel expansion, signal conditioning, and digital I/O accessories and how to connect them to your KPCI-3108 board. Each of these accessories interfaces to your board through a specially-designed adapter/screw-terminal accessory. The following topics are covered:
  - Connecting EXP-1800 channel-expansion accessories to the KPCI-3108 board via an STA-3108-A1 accessory
  - Connecting an MB-01, MB-05, or STA-MB signal conditioning accessory to the KPCI-3108 board via an STA-3108-A2 accessory
  - Connecting an MB-02 signal conditioning/expansion accessory to the KPCI-3108 board via an STA-3108-A3 accessory
  - Connecting digital I/O accessories to the KPCI-3108 board via an STA-3108-D1 accessory

NOTE *When using combination adapter/screw-terminal accessories (STA-3108-A1, STA-3108-A2, STA-3108-A3, or STA-3108-D1) as recommended in these subsections, wire to the screw terminals with caution. Be aware of the following:*

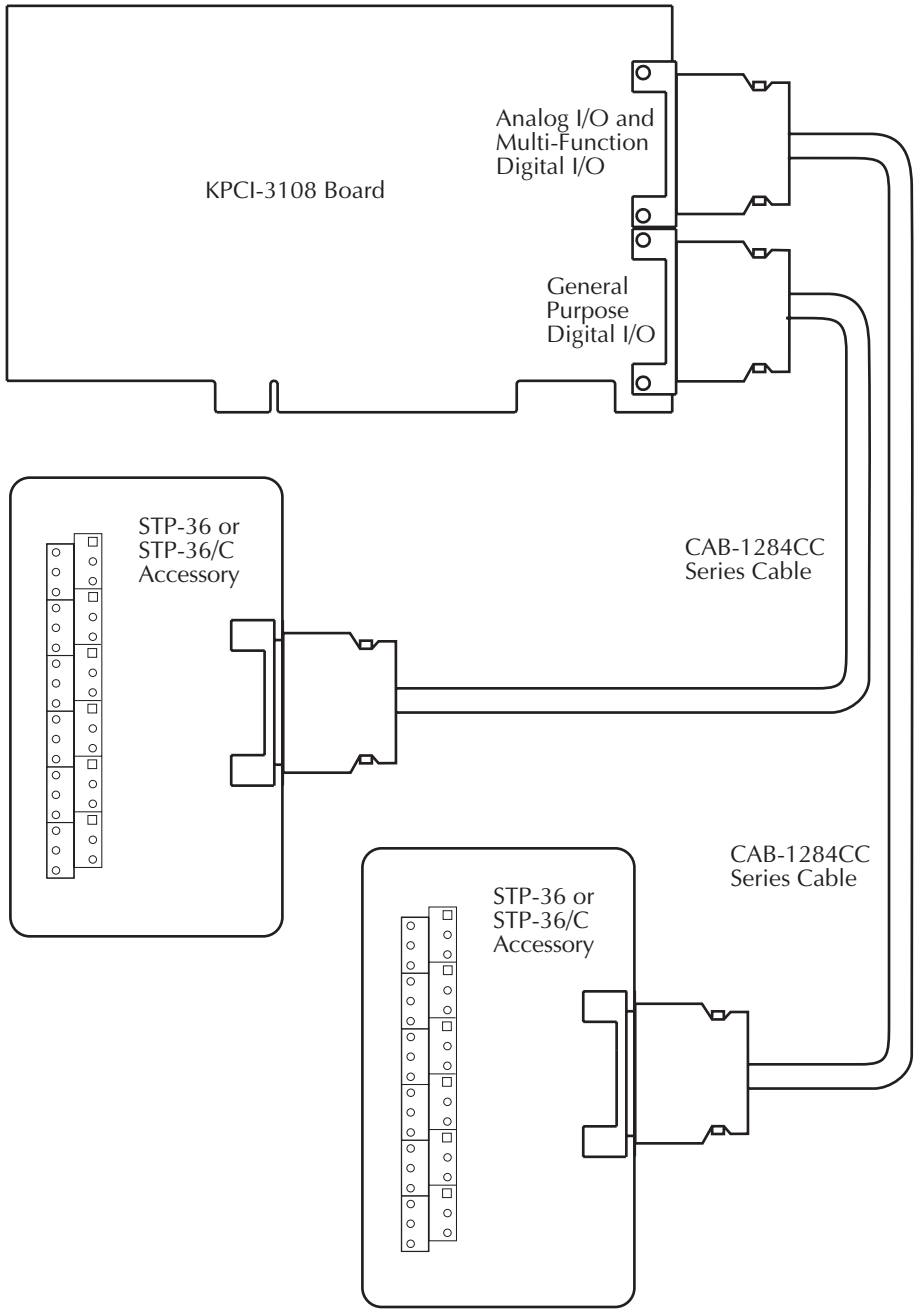
- *All of the screw terminals are connected to the same-numbered pins of a KPCI-3108 "Analog" or "Digital" I/O connector.*
- *When a channel-expansion, signal-conditioning, or digital I/O accessory(s) is connected to the adapter/screw-terminal accessory, some of KPCI-3108 I/O signals at these screw terminals are shared. In general, do not wire external circuits to screw terminals that are shared. However, which screw terminals are actually shared depends on the configuration of the channel-expansion, signal-conditioning, or digital I/O accessory configuration. For example:*
  - *Each EXP-1800 expansion accessory or MB-02 expansion/signal-conditioning accessory is connected to only one single-ended analog input channel. Therefore, if the number of EXP-1800 or MB-02 accessories connected to your board is "n," as many as (16- n) single-ended channels or (8 -n/2) differential channels, are not shared. Unshared channels may be wired to external circuits at the screw terminals. However, be aware that at least four multi-function digital outputs (five for the EXP-1800) are always used for multiplexing and are therefore always shared.*
  - *The MB-01 and MB-05 signal-conditioning accessory and the PB-24, PB-24SM, SSI0-24, and ERB-24 digital I/O accessories each accommodate up to 24 plug-in modules. If you plug in fewer than 24 modules, the analog I/O channels or digital I/O bits not associated with modules are not shared and may be wired to external circuits at the screw terminals.*
  - *Even if filled with plug-in modules, an MB-05 signal-conditioning accessory never shares all analog I/O channels and none of the digital I/O accessories ever shares all digital I/O bits. The remaining channels/bits may be wired to external circuits at the screw terminals.*

Before wiring external circuits, first review your configuration and the instructions for your accessories. Also review the pin-to-pin correspondence between the KPCI-3108 I/O connector and the adapter connector of your adapter/screw-terminal accessory, as it applies to your configuration. Pin-to-pin data is listed in one of the following tables: Table 3-5, Table 3-7, or Table 3-10.

Connecting an STP-36 or STP-36/C screw terminal accessory to a KPCI-3108 board

The STP-36 and STP-36/C accessories provide basic screw terminal wiring to the I/O connector of a KPCI-3108 board. All of the screw terminals are connected to the same-numbered pins of a KPCI-3108 "Analog" or "Digital" I/O connector. Figure 3-4 shows how the accessory connects to the board.

Figure 3-4
Connecting STP-36 and STP-36/C screw terminal accessories



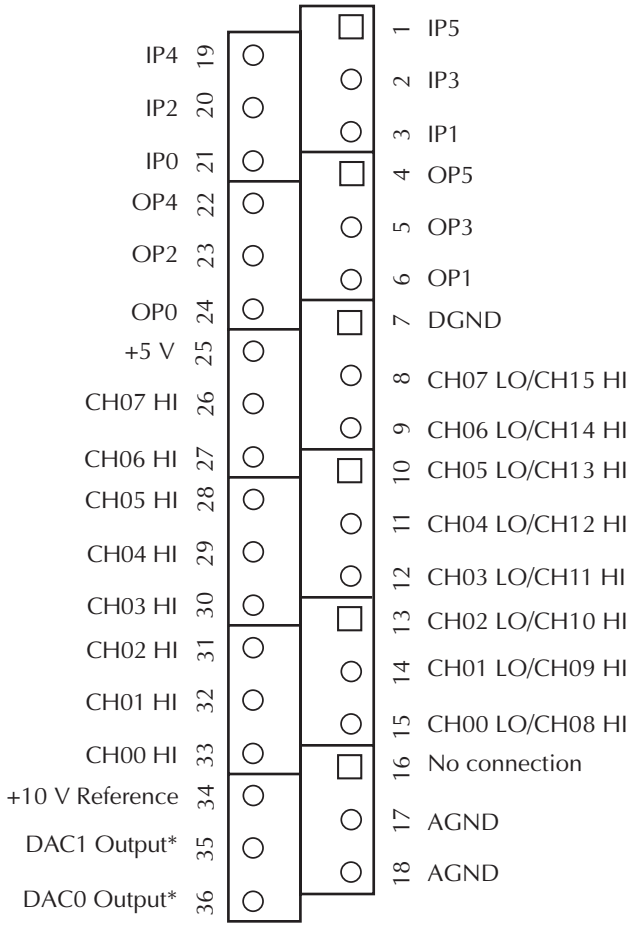
As shown in Figure 3-4 , use a CAB-1284CC Series cable to connect a STP-36 accessories to a KPCI-3108. Available CAB-1284CC Series cables are listed in Table 3-3.

Table 3-3
CAB-1284CC Series cables

Cable	Description
CAB-1284CC-1	IEEE-1284 type C-C round cable with shielded, twisted-pair conductors and molded, 36-pin mini-Centronics connectors on each end. Length is1m.
CAB-1284CC-2	Same as CAB-1284CC-1, except length is 2m.

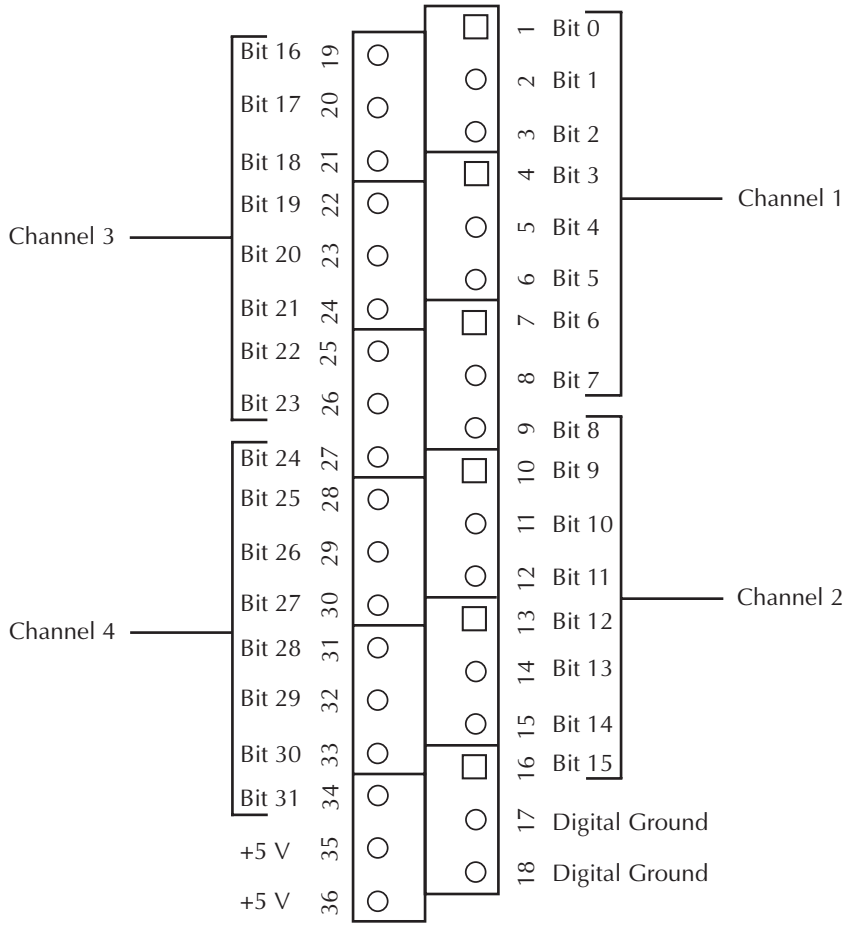
The screw terminal numbers and assignments on an STP-36 or STP-36/C accessory are identical to the pin numbers and assignments on the KPCI-3108 I/O connector to which it is connected. Therefore, when you connect an STP-36 or STP-36/C to the upper "Analog" connector of a KPCI-3108 board, the screw terminal assignments are as shown in Figure 3-5. When you connect an STP-36 or STP-36/C to the lower "Digital" connector of a KPCI-3108 board, the screw terminal assignments are as shown in Figure 3-6. For descriptions of these pins and assignments, refer to Table 3-1 and Table 3-2 under "Identifying I/O connector pin assignments for KPCI-3108."

Figure 3-5
Upper "Analog" screw terminal assignments



*Not available when connected to KPCI-3107.

Figure 3-6
Lower "Digital" screw terminal assignments



Connecting EXP-1800 channel-expansion accessories to the KPCI-3108 board via an STA-3108-A1 accessory

Using one or more EXP-1800 channel expansion accessories—in conjunction with an STA-3108-A1 adapter/screw-terminal accessory—allows you to connect groups of 16 analog inputs to each single-ended input of your KPCI-3108 board. Figure 3-7 and Table 3-4 provide the information you need to interconnect these accessories. Table 3-5 shows the pin-to-pin correspondence between the pins of the KPCI-3108 "Analog" I/O connector and the pins of the STA-3108-A1 50-pin header.

Figure 3-7
Connecting an EXP-1800 channel-expansion accessory and an STA-3108-A1 accessory

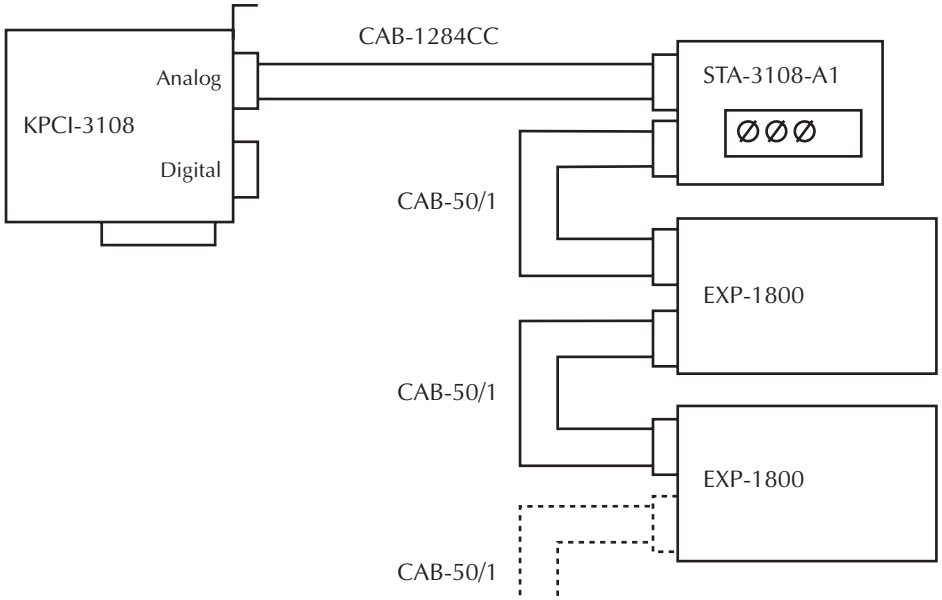


Table 3-4
Connections of EXP-1800 channel-expansion accessory and other accessories needed to a KPCI-3108 board

Channel expansion accessory and required adapter/screw terminal accessory		**Required cables (in addition to CAB-1284CC Series)**		**Additional required accessories**
Accessory	**Description**	**Cable**	**Description**	
EXP-1800	Expansion accessory. Expands one KPCI-3108 single-ended analog input channel into 16 differential analog input channels.	CAB-50/1	Ribbon cable, 18 inches long, with 50-pin headers on each end.	STA-3108-A1 accessory External + 5V power supply for multiple EXP-1800s
STA-3108-A1	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 Series I/O connector to an EXP-1800 channel-expansion accessory, as well as to screw-terminals that are numbered identically to the "Analog" connector pins. A daisy-chain of up to sixteen STA-3108-A1 accessories interfaces the "Analog" KPCI-3108 I/O connector to as many as sixteen EXP-1800 accessories.	CAB-1284CC Series	IEEE 1284 type CC cable; 36-pin mini-Centronics connectors on each end	None

Table 3-5
Pin-to-pin correspondence between upper "Analog" connector and 50-pin accessory

At "Analog" I/O connector		At STA-3108-A1 50-pin header	
Pin number	**Assignment**[1]	**Pin number**	**Assignment**[2]
1	IP5	Not mapped	
2	IP3	Not mapped	
3	IP1	Not mapped	
4	OP5	Not mapped	
5	OP3	45	MUX7 [3]
6	OP1	43	MUX5 [3]
7	DGND	49	GNDD
8	CH07 LO/CH15 HI	17	CH15/CH7 LO
9	CH06 LO/CH14 HI	15	CH14/CH6 LO
10	CH05 LO/CH13 HI	13	CH13/CH5 LO
11	CH04 LO/CH12 HI	11	CH12/CH4 LO
12	CH03 LO/CH11HI	9	CH11/CH3 LO
13	CH02 LO/CH10 HI	7	CH10/CH2 LO
14	CH01 LO/CH09 HI	5	CH9/CH1 LO
15	CH00 LO/CH08 HI	3	CH8/CH0 LO
16	No connection	Not mapped	
17	AGND	25	GNDA
18	AGND	26	GNDA
19	IP4	Not mapped	
20	IP2	Not mapped	
21	IP0	Not mapped	
22	OP4	28	GEXT [3]
23	OP2	46	MUX6 [3]
24	OP0	44	MUX4 [3]
25	+5 V	47	+5V
26	CH07 HI	16	CH7
27	CH06 HI	14	CH6
28	CH05 HI	12	CH5
29	CH04 HI	10	CH4
30	CH03 HI	8	CH3
31	CH02 HI	6	CH2
32	CH01 HI	4	CH1
33	CH00 HI	2	CH0
34	+10V Reference	Not mapped	
35	DAC1 Output[4]	22	ODAC1
36	DAC0 Output[4]	20	ODAC2

[1] Refer also to Table 3-1 for I/O descriptions.
[2] Assignments are based on signal names at the EXP-1800 50-pin header.
[3] The KPCI-3108 board does not output MUX signals from OP0 through OP-4 in all software modes. When using the EXP-1800, these outputs must be configured for MUX control.
[4] This feature is not included with the KPCI-3107 board.

Connecting an MB-01, MB-05, or STA-MB signal conditioning accessory to the KPCI-3108 board via an STA-3108-A2 accessory

Using an MB-01, MB-05, or STA-MB signal conditioning accessory—in conjunction with an STA-3108-A2 adapter/screw-terminal accessory—you can interface signals to your analog inputs through a variety of signal conditioning modules. These modules allow you to connect thermocouples, RTDs, strain gages, voltage-to-frequency converters, etc. to your KPCI-3108 board. Figure 3-8 and Table 3-6 provide the information you need to interconnect MB-01, MB-05, or STA-MB accessories. Figure 3-9 provides the information you need for connecting an STA-MB signal-conditioning accessory and an STA-3108-A2 accessory. Table 3-7 shows the pin-to-pin correspondence between the pins of the KPCI-3108 "Analog" I/O connector and the pins of the STA-3108-A2 37-pin connector.

Figure 3-8
Connecting an MB-01 or MB-05 signal-conditioning accessory and an STA-3108-A2 accessory

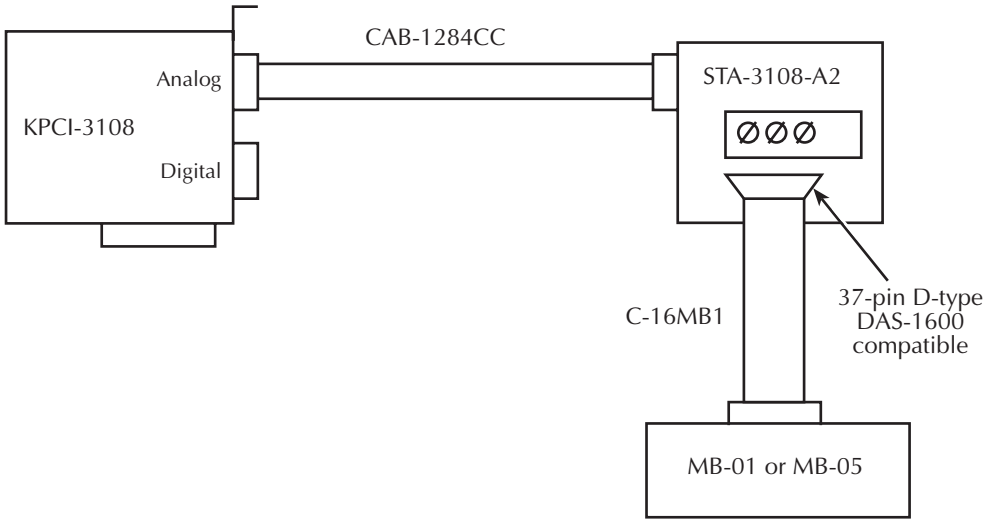


Figure 3-9
Connecting an STA-MB signal-conditioning accessory and an STA-3108-A2 accessory

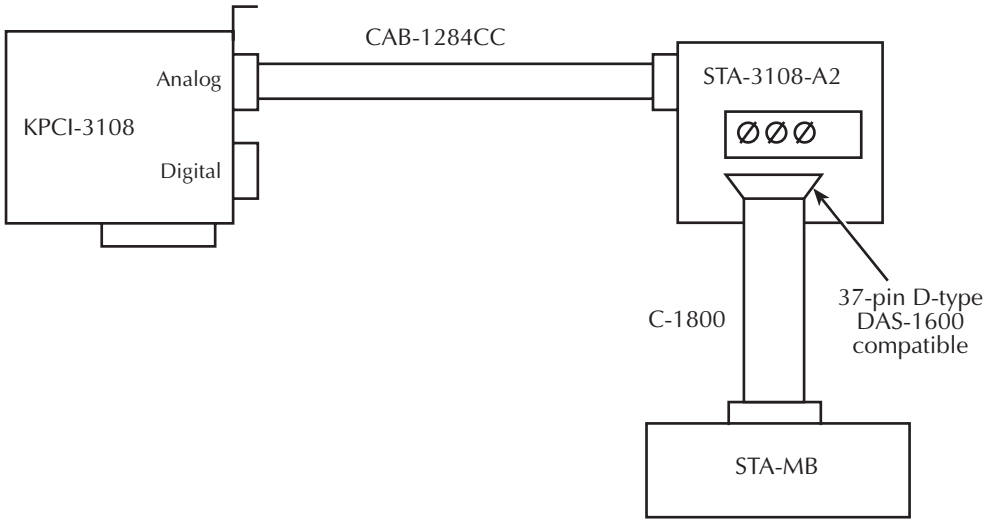


Table 3-6
Connections of accessories to a KPCI-3108 board

Signal-conditioning accessories and required adapter/screw-terminal accessory			Required cables (in addition to CAB-1284CC Series)		Other required accessories
Accessory		**Description**	**Cable**	**Description**	
Signal-conditioning	MB-01	Signal-conditioning module rack. Accommodates up to sixteen MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.	C-16MB1	Cable with a 37-pin female D-type connector on one end and a 26-pin header connector on the other end	STA-3108-A2 accessory External + 5V power supply.
	MB-05	Signal-conditioning module rack. Accommodates up to eight MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.	C-16MB1		
	STA-MB	Signal-conditioning module box/screw-terminal accessory. Accommodates up to four MB Series modules. Each module is connected to one single-ended analog input channel of a KPCI-3108 board.	C-1800	Ribbon cable, 18 in. long, with a 37-pin female D-type connector on each end	STA-3108-A2 accessory
Adapter/screw-terminal	STA-3108-A2	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 Series I/O connector to MB-01, MB-05, and STA-MB signal-conditioning accessories, as well as to screw-terminals that are numbered identically to the "Analog" connector pins.	CAB-1284CC Series	IEEE 1284 type CC cable with 36-pin mini-Centronics connectors on each end	None

*Usable with analog input modules only.

Table 3-7
Pin-to-pin correspondence between upper "Analog" connector and 37-pin connector

At "Analog" I/O connector		At 37-pin connector	
Pin number	**Assignment**[1]	**Pin number**	**Assignment**[2]
1	IP5	Not mapped	
2	IP3	5	IP3
3	IP1	6	IP1/XTRIG
4	OP5	2	CTR0 OUT
5	OP3	3	OP3
6	OP1	4	OP1
7	DGND	7	POWER GND
8	CH07 LO/CH15 HI	11	CH15/CH7 LO
9	CH06 LO/CH14 HI	12	CH14/CH6 LO
10	CH05 LO/CH13 HI	13	CH13/CH5 LO
11	CH04 LO/CH12 HI	14	CH12/CH4 LO
12	CH03 LO/CH11HI	15	CH11/CH3 LO
13	CH02 LO/CH10 HI	16	CH10/CH2 LO
14	CH01 LO/CH09 HI	17	CH9/CH1 LO
15	CH00 LO/CH08 HI	18	CH8/CH0 LO
16	No connection	Not mapped	
17	AGND	19	LL GND
18	AGND	28, 29	LL GND
19	IP4	24	IP2/CTR0 GATE
20	IP2	21	CTR0 CLOCK IN
21	IP0	25	IP0/EXT CLK
22	OP4	Not mapped	
23	OP2	22	OP2
24	OP0	23	OP0
25	+5 V	1	+5 PWR
26	CH07 HI	30	CH7
27	CH06 HI	31	CH6
28	CH05 HI	32	CH5
29	CH04 HI	33	CH4
30	CH03 HI	34	CH3
31	CH02 HI	35	CH2
32	CH01 HI	36	CH1
33	CH00 HI	37	CH0
34	+10 V Reference[3]	Not mapped	
35	DAC1Output[4]	27	DAC1 OUT
36	DAC0 Output[4]	9	DAC0 OUT
Not mapped		8	VREF (-5) [3]
Not mapped		10	DAC0 IN
Not mapped		20	CTR 2 OUT
Not mapped		26	DAC1 IN[5]

[1] Refer also to Table 3-1 for I/O descriptions.
[2] Assignments, based on DAS-1600 signal names, are not meaningful in some software modes; the KPCI-3108 board does not necessarily fully emulate a DAS-1600.
[3] The 37-pin connector VREF (-5) is not connected to +10V ref., due to voltage differences.
[4] This feature is not included with the KPCI-3107 board.
[5] A KPCI-3108 board does not use multiplying DACs, so it does not support DAC IN.

Connecting an MB-02 signal conditioning/channel-expansion accessory to the KPCI-3108 board via an STA-3108-A3 accessory

Using one MB-02 signal conditioning/channel-expansion accessory—in conjunction with an STA-3108-A3 adapter/screw-terminal accessory—you can do the following:

- Signal-condition up to sixteen analog signals through a variety of signal conditioning modules. The modules allow you to connect thermocouples, RTDs, strain gages, voltage-to-frequency converters, etc., to your KPCI-3108 board.
- Expand the input capacity of your board. The MB-02 multiplexes the sixteen conditioned signals to one single-ended input of your KPCI-3108 board.

You can connect up to four MB-02 accessories to each STA-3108-A3 accessory. Further, you can daisy-chain up to four STA-3108-A3 accessories together. Therefore, it is possible to signal condition and connect up to 256 analog signals to one KPCI-3108 board.

Figure 3-10 and Table 3-8 provide the information you need to interconnect MB-02 accessories. Refer to the packing list included with your STA-3108-A3 accessory for pin-to-pin correspondence between the pins of the KPCI-3108 "Analog" I/O connector and the pins of the four STA-3108-A3 26-pin headers.

Figure 3-10
Connecting MB-02 signal-conditioning/channel-expansion accessories and an STA-3108-A3 accessory

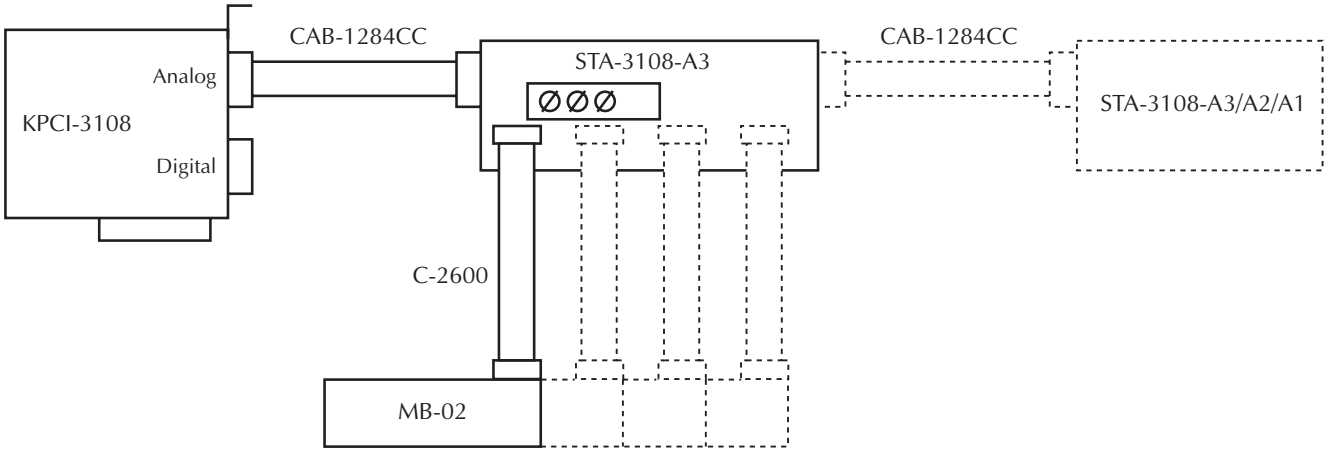


Table 3-8
Connections of the MB-02 signal-conditioning/channel-expansion accessory and other accessories needed to a KPCI-3108 board

Signal-conditioning/channel-expansion accessory and required adapter/screw-terminal accessory		**Required cables (in addition to CAB-1284CC Series)**		**Additional required accessories**
Accessory	**Description**	**Cable**	**Description**	
MB-02	Signal-conditioning-module/channel-expansion rack. Accommodates up to sixteen MB Series modules. All sixteen modules are multiplexed to one single-ended analog input channel of a KPCI-3108 board.	C-2600 One required for each MB-02 rack	Ribbon cable, 18 inch, with a 26-pin header connector at each end (and one in the middle, not used in the recommended configuration)	STA-3108-A3 accessory External + 5V power supply.
STA-3108-A3	Adapter/screw-terminal accessory. Interfaces the "Analog" KPCI-3108 I/O connector to as many as four MB-02 accessories, as well as to screw-terminals that are numbered identically to the "Analog" connector pins. A daisy-chain of up to four STA-3108-A3 accessories interfaces the "Analog" KPCI-3108 I/O connector to as many as sixteen MB-02 accessories.	CAB-1284CC Series	IEEE 1284 type CC cable; 36-pin mini-Centronics connectors on each end	None

Connecting digital I/O accessories to the KPCI-3108 board via an STA-3108-D1 accessory

Using one of the following digital I/O accessories—in conjunction with an STA-3108-D1 adapter/screw-terminal accessory—you can input and/or output optically-isolated AC and DC digital signals or output relay contact closures with your KPCI-3108 board.

- PB-24
- PB-24SM
- SSIO-24
- ERB-24
- SRA-01
- ERA-01
- STA-3108-D1

Figure 3-11 and Table 3-9 provide the information you need to connect these accessories to your board. Table 3-10 shows the pin-to-pin correspondence between the pins of the KPCI-3108 "Digital" I/O connector and the pins of the STA-3108-D1 50-pin header.

Figure 3-11
Connecting digital I/O accessories and an STA-3108-D1 accessory

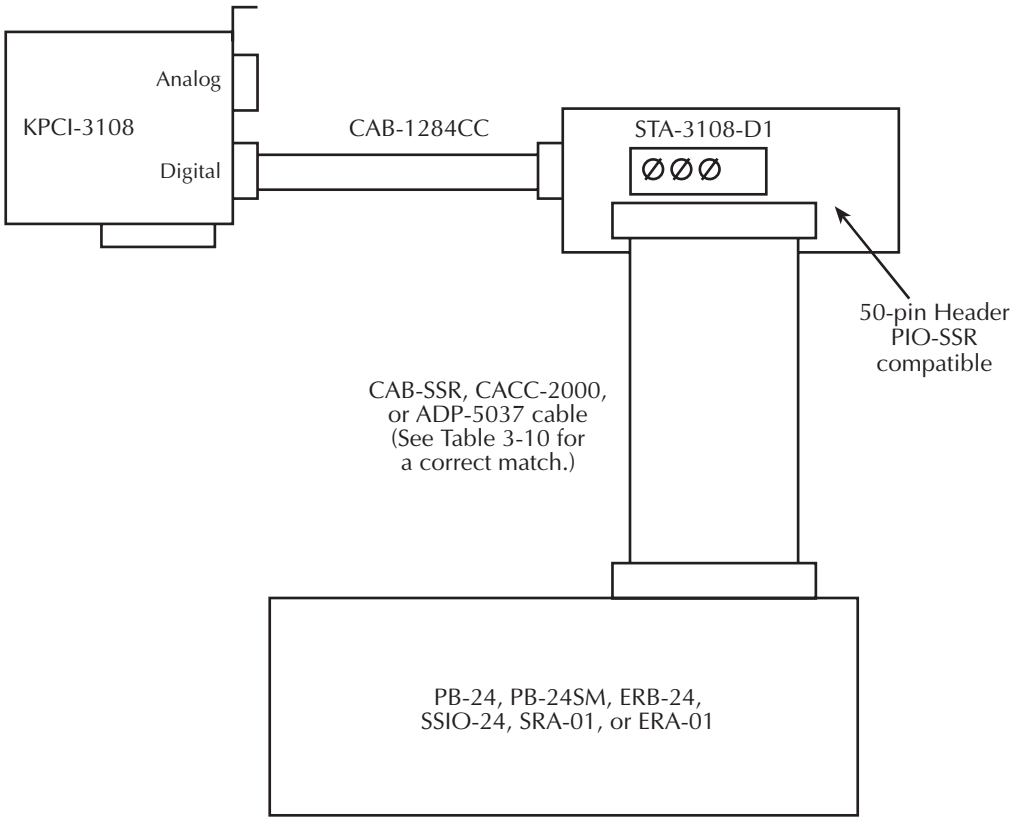


Table 3-9
Digital I/O accessories and required connection accessories

Digital I/O accessories and required adapter/screw-terminal accessory			Required cables (in addition to CAB-1284CC Series)		Additional required accessories
Accessory		Description	Cable	Description	
Digital I/O	PB-24	Industry-standard baseboard that accommodates 24 standard-size solid-state relay modules.	CAB-SSR	Ribbon cable, 3 ft, that connects PB-24 or PB-24SM to a 50-pin header	STA-3108-D1 accessory
	PB-24SM	Industry-standard baseboard that accommodates 24 miniature SM Series solid-state relay modules.			
	SSIO-24	Module interface board that accommodates up to 24 miniature, optically-isolated solid-state digital I/O modules	CACC-2000	Ribbon cable, 24 in, with 50-pin female connector on each end	STA-3108-D1 accessory
	ERB-24	Relay board with 24 double-pole, double-throw (dual Form C) electromechanical relays			
	SRA-01	Module interface board, in box, that accommodates up to eight industry-standard solid-state digital I/O modules	ADP-5037	Conversion cable with a 50-pin connector at one end and a small box, terminating in a 37-pin D-type connector, at the other end	STA-3108-D1 accessory
	ERA-01	Relay board, in box, with eight single-pole, double-throw (Form C) electromechanical relays			
Adapter/screw-terminal	STA-3108-D1	Adapter/screw-terminal accessory. Interfaces the "Digital" KPCI-3108 Series I/O connector to a PB-24, PB-24SM, ERB-24, SSIO-24, SRA-01, or ERA-01 digital I/O accessory, as well as to screw-terminals that are numbered identically to the "Digital" connector pins.	CAB-1284CC Series	IEEE 1284 type CC cable; 36-pin mini-Centronics connectors on each end	None

Table 3-10
Pin-to-pin correspondence between lower "Digital" I/O connector and 50-pin accessory

At KPCI-3108 "Digital" I/O connector		At STA-3108-D1 50-pin header	
Pin number	**Assignment (Refer also to Table 3-2 for I/O descriptions)**	**Pin number**	**Assignment**
1	Bit 0	15	PA0
2	Bit 1	13	PA1
3	Bit 2	11	PA2
4	Bit 3	9	PA3
5	Bit 4	7	PA4
6	Bit 5	5	PA5
7	Bit 6	3	PA6
8	Bit 7	1	PA7
9	Bit 8	47	PB0
10	Bit 9	45	PB1
11	Bit 10	43	PB2
12	Bit 11	41	PB3
13	Bit 12	39	PB4
14	Bit 13	37	PB5
15	Bit 14	35	PB6
16	Bit 15	33	PB7
17	DGND	All even- numbered pins	Digital common
18	DGND		Digital common
19	Bit 16	31	PC0
20	Bit 17	29	PC1
21	Bit 18	27	PC2
22	Bit 19	25	PC3
23	Bit 20		
24	Bit 21		
25	Bit 22		
26	Bit 23		
27	Bit 24		
28	Bit 25		
29	Bit 26		
30	Bit 27		
31	Bit 28	23	PC4
32	Bit 29	21	PC5
33	Bit 30	19	PC6
34	Bit 31	17	PC7
35	+5V	49	+5V
36	+5V		

Wiring analog input signals

This section provides general guidance on wiring your circuits to single-ended and differential inputs, as well as special precautions to avoid problems when wiring signals to a KPCI-3108 set for high gains.

WARNING **Do NOT connect data acquisition inputs to the AC line. Keep data acquisition cables and connections away from any AC line connections. Interconnections or shorting between data and power lines can result in personal injury or death or extensive damage to your computer. To prevent this problem, do the following:**

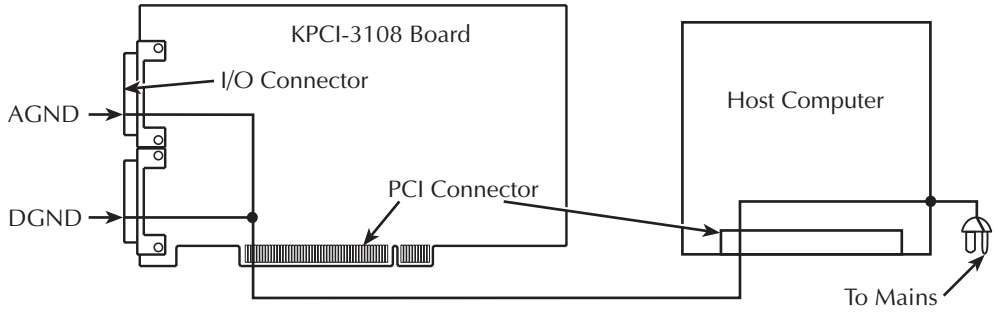
- **Avoid direct connections to the AC line by using safety approved isolation transformers, isolation amplifiers, or both.**
- **Ensure that all connections are tight and sound, so that signal wires are unlikely to come loose and short to hazardous voltages.**

CAUTION **Ensure that both the computer and the external circuits are turned OFF before making any connections. Making connections while the computer and external circuits are powered can damage the computer, the board, and the external circuit.**

Ensure that no analog-input signal exceeds ±15V, which is the maximum allowable rating for the board. Exceeding ±15V will damage the board.

NOTE *KPCI-3108 boards contain separate ground connections for analog and digital signals. Use the analog ground (AGND) for analog signals and analog power; use the digital ground (DGND) for digital signals and other power-supply returns. Do this to avoid interference from digital switching noise currents on sensitive analog signals. However, be aware that both analog and digital grounds are tied together at the board PCI connector and are ultimately connected to the building system ground via the mains. See Figure 3-12. I/O connector pin assignments and descriptions for AGND and DGND are provided in Figure 3-2, Figure 3-3, Table 3-1, and Table 3-2.*

Figure 3-12
Analog and digital ground path



NOTE *Though the circuit diagrams show direct connections to channel input pins of the main I/O connector, you must make actual connections through the corresponding screw terminals of an STP-36 Series accessory or through EXP-1800 or MB Series expansion/signal-conditioning accessories and unshared terminals of the required STA-3108-A Series accessory.*

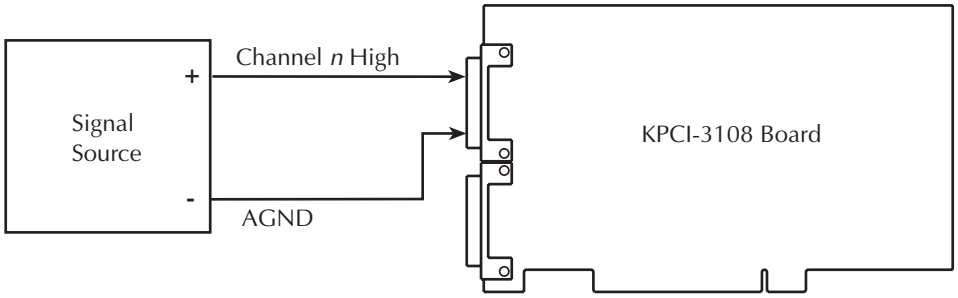
The circuit diagrams in this section represent wiring of a single signal source to a single channel (typically designated as "channel n"). Differential analog circuits can be used with any differential input. Single-ended analog circuits can be used with any single-ended input.

Wiring a signal to a single-ended analog input

NOTE *Before wiring your signals to single-ended inputs, ensure that you understand the limitations of single-ended inputs. Refer to Section 2, "Choosing between the differential and single-ended termination modes."*

Figure 3-13 shows the connections between a signal source and one channel of a KPCI-3108 board configured for single-ended input mode.

Figure 3-13
Wiring a signal source to a board configured for single-ended inputs



Wiring a floating signal source to a differential analog input

NOTE *If you are unclear about whether to use differential or single-ended input mode, refer to Section 2, "Choosing between the differential and single-ended termination modes."*

Figure 3-14 shows three connection schemes for wiring a signal source to a KPCI-3108 channel when the board is configured for differential input and the input signal source is floating.

Floating signal sources are ideally either totally ungrounded (a battery, for example) or are otherwise not connected either directly or indirectly to the building ground or analog signal ground. (Real floating signal sources do have finite, though small, coupling to ground due to finite insulation resistance and other sources of current leakage, such as capacitive coupling in a transformer.) Examples of floating signal sources include devices powered by batteries, devices powered through isolation transformers, ungrounded thermocouples, and outputs of isolation amplifiers. Using floating signal source intrinsically avoids ground loops.

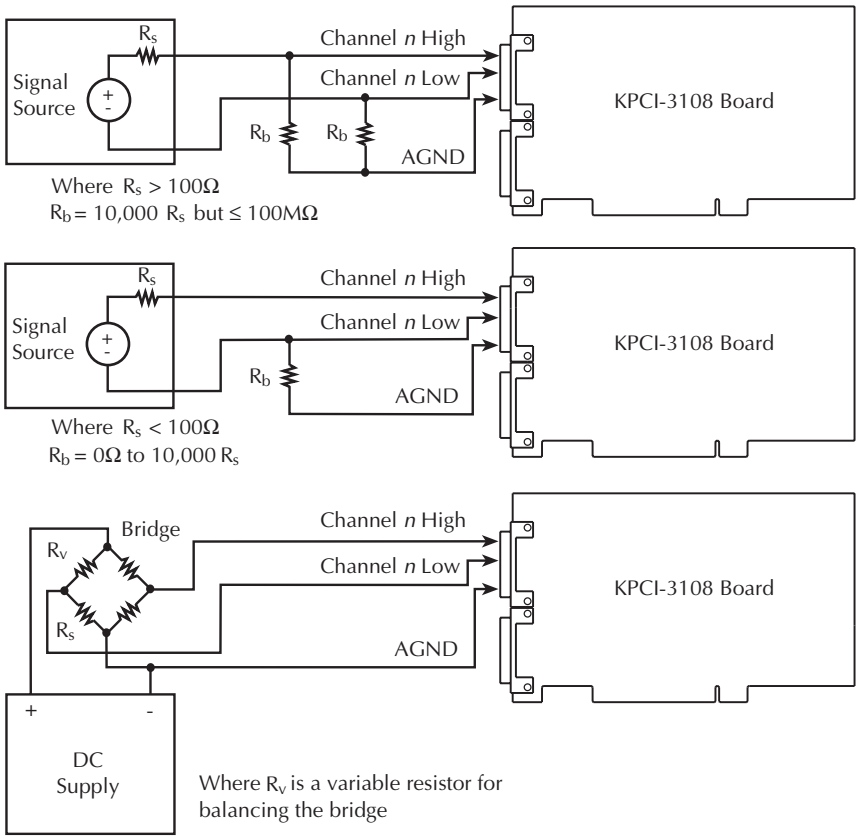
However, when your KPCI-3108 board is used in the differential input mode, a current path must be connected to the analog ground terminal. When the signal source floats, the lack of a ground reference point allows instrumentation amplifier bias currents to raise the common-mode voltage of the signal to high values. Excessive common mode voltages result in excessive signal errors or, worse, amplifier saturation and unusable data.

NOTE *The bias current of the input instrumentation amplifier is a very small but finite current drawn from an input terminal to the amplifier. The magnitude of the bias current depends on the amplifier design and may range from a few femtoamperes to a few microamperes.*

The common-mode voltage (V_{cm}) is a voltage that is common to both the input-high and input-low terminals of a differential input: it appears between each terminal and ground.

If your signal source is floating, you must provide the path to the analog ground. Use one or two bias return resistors, as discussed below and illustrated in Figure 3-14.

Figure 3-14
Wiring a floating signal source to differential inputs: three common examples



The minimum bias return resistance and the number of bias resistors (one or two) are determined by noise considerations. The maximum bias return resistance (R_b) is limited by the maximum acceptable common-mode voltage that occurs due to the bias current, as follows:

Common-mode voltage due to bias current = (Bias current) * (Bias return resistance, R_b)

The remaining discussions of this section guide you in selecting bias return resistors.

Using a single bias return resistor (middle circuit of Figure 3-14). If the signal source resistance (RS) is low, one bias return resistor connected between the input-low terminal and the analog ground is adequate.

The minimum bias return resistance is determined by the signal source resistance and the susceptibility and exposure of your circuit to noise pickup from the environment. If the source resistance (R_S) is low, the bias resistance can generally be low. In some cases, the bias resistance (R_b) can be zero. That is, you can connect a lead directly between the analog ground and the negative terminal of the signal source. However, the following then occurs:

- Electrostatically-coupled noise in the negative signal lead is shunted directly to ground and does not affect the negative signal input.
- Electrostatically-coupled noise in the positive signal lead is not shunted directly to ground and causes a net noise voltage at the positive signal input.

The net voltage at the positive signal input cannot be rejected by the common-mode rejection capabilities of the KPCI-3108.

Therefore, depending on the source resistance (R_S) and/or the electrostatic noise pickup, it is frequently better to use a larger bias resistance (R_b) to help balance the ground return paths of the positive and negative signals. The higher resistance makes the ground paths and noise coupling in the positive and negative signals more similar. The noise that is common to both positive and negative signals can then be rejected as part of the common mode voltage. If the source resistance is less than 100 ohms, you may select the bias return resistance as follows:

Bias return resistance, R_b = 10,000 * (Source resistance, R_S) if $R_S < 100\Omega$

Using two bias return resistors (top circuit of Figure 3-14). You can slightly improve noise rejection by connecting identical bias return resistors to both the positive and negative signals. This balances the ground return paths. Use the following resistance value:

Bias return resistance, R_b = 10,000 * (Source resistance, R_S), 100MΩ max, if $R_S > 100\Omega$

However, be aware that the bias return resistor connected to the input-high terminal loads the signal, causing a proportional error.

Using no bias return resistors with a bridge circuit (bottom circuit of Figure 3-14). In the lower circuit of Figure 3-14, added bias return resistors are not needed. The bridge resistors at the signal source inherently provide the bias current return path. The common mode voltage at the input terminals is the voltage drop across R_S of the bridge.

Wiring a ground-referenced signal source to a differential analog input

NOTE *If you are unclear about whether to use differential or single-ended input mode, refer to Section 2, "Choosing between the differential and single-ended termination modes."*

A ground-referenced signal source is a signal source that is connected directly or indirectly to the building system ground. The analog signal ground of the KPCI-3108 is ultimately connected to the building system ground via the power mains, as shown in Figure 3-12. Therefore, the ground-referenced signal source is also indirectly connected to the analog ground.

However, the quality of the ground connection between the signal source and analog ground of the KPCI-3108 may be poor. The signal-source ground and the KPCI-3108 board analog ground are typically not at the same voltage level. This voltage difference is due to the wiring between the data acquisition equipment and the building system ground, to which power-using and noise-generating equipment is typically also connected. The voltage difference is seen at the KPCI-3108 differential input terminals as a common-mode voltage (V_{cm}), so called because it is effectively common to both the input-high and input-low terminals. An ideal, properly connected differential input responds only to the difference in the signals at the input-high and input-low terminals. The common-mode voltage is rejected, leaving only the desired signal. Practically, the common-mode voltage always causes an error, typically small, that is limited by the common-mode rejection ratio (CMRR) of the differential input.

Figure 3-15 illustrates how to satisfactorily connect a ground-referenced signal source to a differential input. In the upper circuit of Figure 3-15, a separate ground return line is connected between the negative-terminal ground of the signal source and the analog ground of the KPCI-1800HC Series board. Because both the input-high and input-low terminals of the KPCI-1800HC have high input impedance, effectively all ground currents due to ground voltages flow through the separate ground-return line. Because the separate ground return line is common to both the input-high and input-low terminals, the voltage drop across it is rejected as a common-mode voltage.

In the lower circuit of Figure 3-15, the grounding connection for a bridge circuit powered by a ground-referenced power supply is the same as for a floating bridge. When the bridge has a ground-referenced power supply, the common mode voltage is the sum of the voltage drop across the ground line and the voltage drop across R_S of the bridge.

Figure 3-15
Satisfactory differential input connections that avoid a ground loop with ground-referenced signals

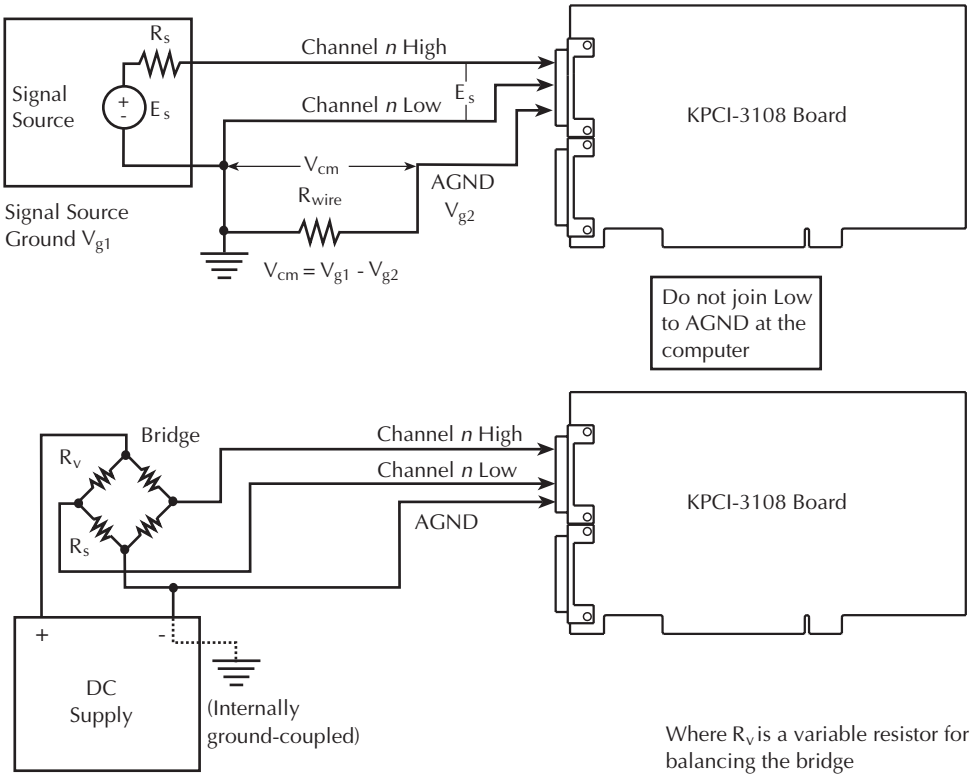
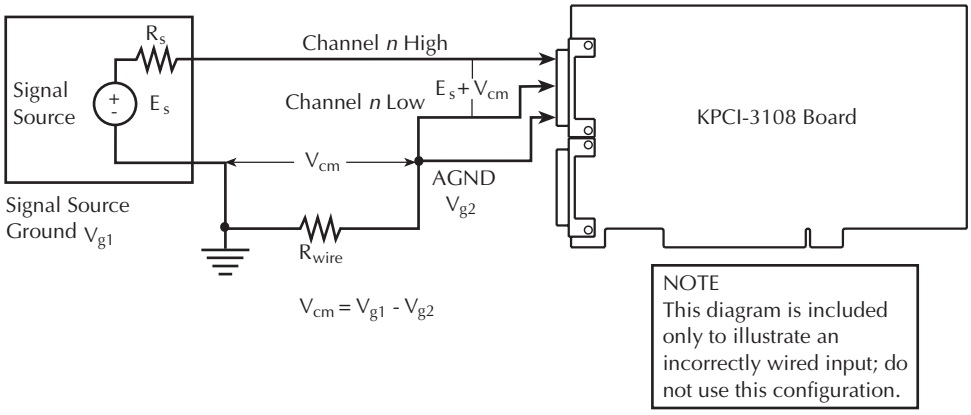


Figure 3-16 illustrates how NOT to connect a differential input. If the analog ground and input-low terminal of the KPCI-3108 board are joined near the board, a ground loop current flows in the negative signal lead. The voltage difference across this signal lead is then a component of the measured signal, not a common-mode voltage. A differential amplifier cannot reject this unwanted signal component.

Figure 3-16
Improper differential input connection, which creates a ground loop error



Avoiding wiring problems at high gains

Operating a KPCI-3108 board at a gain of 200 or more can lead to problems if your application is unable to cope with noise. If special precautions are not taken, the high gain, high speed, and large bandwidth of this board allow thermal emfs and noise to easily degrade performance. The following suggestions are provided to help you to minimize problems at high gain.

- Connect low-level signals to inputs configured as differential inputs. Inputting signals at high gains in single-ended mode introduces enough ground-loop noise to produce large fluctuations in readings.
- Minimize noise from crosstalk and induced-voltage pickup in cables and screw-terminal accessories. Use shielded cables for low level signals whenever possible. Induced noise from radio frequency (RF) and magnetic fields can easily exceed tens of microvolts, even on one-foot or two-foot long cables. Shielded cable helps to avoid this problem.The CAB-1284CC Series cables (or standard IEEE 1284 Type C-C mini-Centronics cables) that are used to connect accessories directly to KPCI-3108 I/O connectors are shielded, and signals to differential inputs are conducted through twisted pairs. Nonetheless, minimize the length of CAB-1284CC Series cables to minimize interferences.Connect cable shields to the analog ground (AGND) and the inner conductors to the input low (LO) and input-high (HI) terminals. Channel LO and AGND should have a common DC return (or connection) at some point; this return should be as close to the signal source as possible.
- Avoid bimetallic junctions in the input circuitry. For example, the thermal emf of a Kovar-to-copper junction, such as at the Kovar leads of reed relay, is typically 40µV/˚C. Thermal emfs at bimetallic junctions, combined with air currents and other sources of temperature variation, can introduce strange random signal variations.
- Consider filtering, which can be accomplished with hardware (resistors, capacitors, and so on) but is often accomplished more easily with software. Instead of reading the channel once, read it 10 or more times in quick succession and average the readings. If the noise is random and Gaussian, it will be reduced by the square root of the number of readings.

Refer also to Section 2, "Optimizing throughput," for additional precautions about assigning high gains to channels in the channel-gain queue.

Wiring analog output signals (KPCI-3108 board only)

This section provides a few guidelines on wiring the analog outputs from the two 16-bit DACs (digital-to-analog converters) that are available on a KPCI-3108 board. Each DAC can be software-configured to output a range of ±10V, ±5V, 0 to 10V, or 0 to 5V. Performance characteristics and drive capabilities for these DACs are listed in Appendix A.

WARNING **Do NOT intersperse data acquisition connections with AC line connections. Keep data acquisition cables and connections away from any AC line connections. Interconnections or shorting between data and power lines can result in personal injury or death or extensive damage to your computer. To prevent this problem, ensure that all connections are tight and sound, so that signal wires are unlikely to come loose and short to hazardous voltages.**

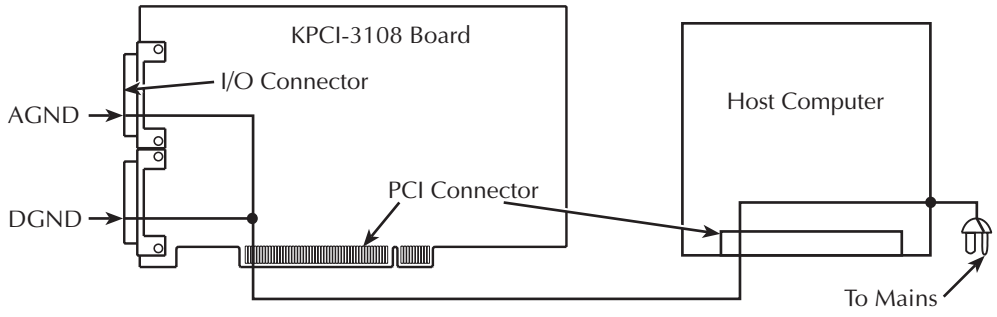
CAUTION **Ensure that both the computer and the external circuit are turned OFF before making any connections. Making connections while the computer and external circuits are powered can damage the computer, the board, and the external circuit.**

Ensure that connected loads do not draw more than 5 mA, the maximum allowable output current for the board.

NOTE *Avoid large capacitive loads at the analog outputs. Capacitive loads higher than 100µF destabilize the analog outputs and make them susceptible to ringing (transient oscillations).*

KPCI-3108 boards contain separate ground connections for analog and digital signals. Use the analog ground (AGND) for analog signals and analog power; use the digital ground (DGND) for digital signals and other power-supply returns. Do this to avoid interference from digital switching noise currents on sensitive analog signals. However, be aware that both analog and digital grounds are tied together at the board PCI connector and are ultimately connected to the building system ground via the mains. See Figure 3-17. I/O connector pin assignments and descriptions for AGND and DGND are provided in Figure 3-2, Figure 3-3, Table 3-1, and Table 3-2.

Figure 3-17
Analog and digital ground path



You must make all analog output connections to the upper "Analog" I/O connector of the board through one of the following:

- The screw terminals of an STP-36 or STP-36/C screw terminal accessory. To connect an STP-36 or STP-36/C accessory to your board, refer to "Connecting an STP-36 or STP-36/C screw terminal accessory to a KPCI-3108 board" earlier in Section 3.
- Terminals on an MB-02 signal-conditioning/channel-expansion accessory and unshared terminals of the required STA-3108-A Series accessory. Refer to the manual for your MB-02 Series accessory and to "Connecting an MB-02 signal conditioning/channel-expansion accessory to the KPCI-3108 board via an STA-3108-A3 accessory" earlier in Section 3.

The appropriate STP-36, STP-36/C, or STA-3108-A3 screw terminals are identified in Table 3-11.

Table 3-11
Screw terminals used to wire analog outputs of KPC-3108 board

Screw terminal	Assignment	Description
17, 18	AGND	Analog ground
35	DAC1 Output	Analog output from digital-to-analog converter number 1*
36	DAC0 Output	Analog output from digital-to-analog converter number 0*

Wiring digital input and output signals

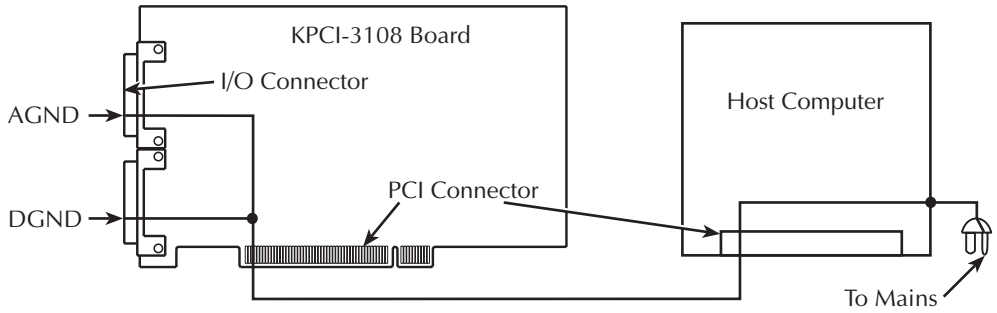
WARNING **Do NOT connect data acquisition inputs to the AC line. Keep data acquisition cables and connections away from any AC line connections. Interconnections or shorting between data and power lines can result in personal injury or death or extensive damage to your computer. To prevent this problem, do the following:**

- **Avoid direct connections to the AC line by using safety approved isolation transformers, isolation amplifiers, or both.**
- **Ensure that all connections are tight and sound, so that signal wires are unlikely to come loose and short to hazardous voltages.**

CAUTION **Ensure that both the computer and the external circuit are turned OFF before making any connections. Making connections while the computer and external circuits are powered can damage the computer, the board, and the external circuit.**

NOTE *KPCI-3108 boards contain separate ground connections for analog and digital signals. Use the analog ground (AGND) for analog signals and analog power; use the digital ground (DGND) for digital signals and other power-supply returns. Do this to avoid interference from digital switching noise currents on sensitive analog signals. However, be aware that both analog and digital grounds are tied together at the board PCI connector and are ultimately connected to the building system ground via the mains. See Figure 3-18. I/O connector pin assignments and descriptions for AGND and DGND are provided in Figure 3-2, Figure 3-3, Table 3-1, and Table 3-2.*

Figure 3-18
Analog and digital ground path



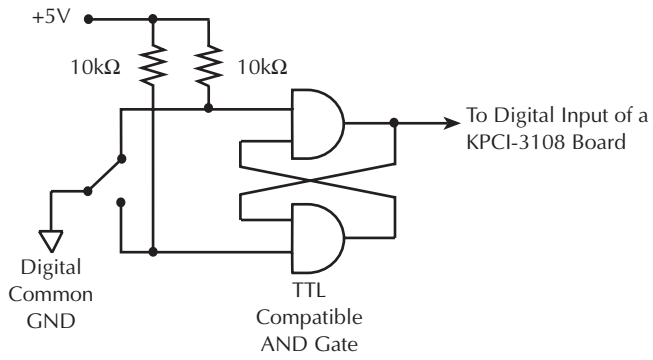
A KPCI-3108 board has two types of digital I/O. The lower "Digital" I/O connector provides 32 high current general-purpose bits. The upper "Analog" I/O connector provides twelve multi-function TTL bits. Following "General wiring considerations for digital I/O," these two types of digital I/O are discussed separately below.

General wiring considerations for digital I/O

For all digital I/O, logic 1 on an I/O line indicates that the input/output is high (greater than 2.0V); logic 0 on an I/O line indicates that the input/output is low (less than 0.8V). The digital inputs are compatible with TTL-level signals. These inputs are provided with 10kΩ pull-up resistors connected to +5V; therefore, the inputs appear high (logic 1) if no signal is connected.

External circuits must properly match the input requirements of the board. Even though the digital inputs of your KPCI-3108 board are already equipped with 10kΩ pull-up resistors, some applications may also require you to eliminate contact bounce at the input. The effects of contact bounce may be eliminated by programming in your application software. However, it is often desirable to eliminate contact bounce from the signal, using a de-bounce circuit between the contacts and the KPCI-3108 input. Figure 3-19 shows a typical de-bounce circuit that can be used with Form C contacts.

Figure 3-19
Contact de-bounce circuit



Wiring general-purpose digital I/O signals

The lower "Digital" I/0 connector provides 32 bits of high current I/O (15 mA max. source, 64 mA max. sink output current). These general-purpose bits are software-configurable as either inputs or outputs in groups of eight—each group of eight bits being handled by one of four eight-bit registers. These bits may be used for a variety of purposes, as for the bits of common digital I/O boards such as the Keithley PIO-24 and KPCI-PIO24 boards. The output current capabilities of these bits are much higher than available from the industry-standard type-8255 digital I/O chip on many commercial digital I/O boards.

Wire a general-purpose digital I/O signal between the appropriate digital I/O pin and a digital ground pin on your KPCI-3108 board. Make all connections to the lower "Digital" I/O connector of the board through one of the following:

- Connect all I/O through the screw terminals of an STP-36 or STP-36/C screw terminal accessory. Refer to "Connecting an STP-36 or STP-36/C screw terminal accessory to a KPCI-3108 board."
- Terminals on any of six compatible digital I/O accessories and unshared terminals of the required STA-3108-D1 accessory. Refer to the manual for your digital I/O accessory and to "Connecting digital I/O accessories to the KPCI-3108 board via an STA-3108-D1 accessory" earlier in Section 3.

The appropriate STP-36, STP-36/C, or STA-3108-D1 screw terminals are identified in Table 3-12.

Table 3-12
Screw terminals used to wire general-purpose digital I/O

Screw terminal	Assignment	Description
1 2 3 : 8	Bit 0 Bit 1 Bit 2 : Bit 7	General-purpose digital I/O bits, channel 0. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
9 10 11 : 16	Bit 8 Bit 9 Bit 10 : Bit 15	General-purpose digital I/O bits, channel 1. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
17, 18	DGND	Digital grounds.
19 20 21 : 26	Bit 16 Bit 17 Bit 18 : Bit 23	General-purpose digital I/O bits, channel 2. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
27 28 29 : 34	Bit 24 Bit 25 Bit 26 : Bit 31	General-purpose digital I/O bits, channel 3. As a group, these 8 bits are user-configurable as either all inputs or all outputs. (The 8 bits comprise the register of a type 652 chip.)
35, 36	+5V	+ 5 VDC from computer bus. (Refer to "Wiring +5V power to external circuits.")

Wiring multi-function digital I/O signals

KPCI-3108 boards provide six digital inputs and six digital outputs at the upper "Analog" I/O connector. These I/O bits are software-configurable to preform a variety of functions, including control of external signal conditioning and expansion accessories.

You must wire all multi-function digital I/O connections to the upper "Analog" I/O connector of the board through one of the following:

- The screw terminals of an STP-36 or STP-36/C screw terminal accessory. Wire a multi-function I/O signal between the appropriate digital I/O terminal and a digital ground terminal. To connect an STP-36 or STP-36/C accessory to your board, refer to "Connecting an STP-36 or STP-36/C screw terminal accessory to a KPCI-3108 board" earlier in Section 3.
- Unshared digital I/O screw terminals of the required STA-3108-A Series accessory, when using an analog signal-conditioning/expansion accessory. Refer to the manual for your signal-conditioning/expansion accessory and to one of the following sections earlier in Section 3:
  - "Connecting EXP-1800 channel-expansion accessories to the KPCI-3108 board via an STA-3108-A1 accessory"
  - "Connecting an MB-01, MB-05, or STA-MB signal conditioning accessory to the KPCI-3108 board via an STA-3108-A2 accessory"
  - "Connecting an MB-02 signal conditioning/channel-expansion accessory to the KPCI-3108 board via an STA-3108-A3 accessory"

Table 3-13 summarizes general STP-36, STP-36/C, or STA-3108-A Series screw terminals used to wire the multi-function digital I/O of the KPC-3108 board. The assignments are ordered numerically according to the identically-numbered pins of a KPCI-3108 upper "Analog" I/O connector.

Table 3-13
Assignments and descriptions for multi-function digital I/O accessories

Screw terminal	Assignment	Description
1 2 3	IP5 IP3 IP1	Multi-function digital input bits, user-configurable for: • Counter/timer timebase or gate inputs • External pacer input for A/D or D/A conversion • External digital trigger • Target-mode digital input
4 5 6	OP5 OP3 OP1	Multi-function digital output bits, user-configurable for: • Counter/timer outputs • Trigger output • Control and/or addressing for EXP-1800 expansion accessories or MB-02 signal conditioning accessories • Pacer clock output • Target-mode digital output
7	DGND	Digital ground.
19 20 21	IP4 IP2 IP0	Multi-function digital input bits, user-configurable for: • Counter/timer timebase or gate inputs • External pacer for A/D or D/A conversion • External digital trigger • Target-mode digital input

Table 3-13
Assignments and descriptions for multi-function digital I/O accessories (cont.)

Screw terminal	Assignment	Description
22 23 24	OP4 OP2 OP0	Multi-function digital output bits, user-configurable for: • Counter/timer outputs • Trigger output • Control and/or addressing for EXP-1800 expansion accessories or MB-02 signal conditioning accessories • Pacer clock output • Target-mode digital output
25	+5 V	+5 VDC from computer bus. (Refer to "Wiring +5V power to external circuits.")

Table 3-14 summarizes specific pin/terminal assignments and descriptions for the multi-functional digital inputs at screw terminals of STP-36, STP-36/C, and STA-3108-A Series accessories. The assignments are ordered numerically according to the assigned bits.

Table 3-14
Bit assignments and descriptions for multi-function digital inputs

Bit assignment	Screw terminal	Description
IP0	21	Configurable as one of the following: • XPCLK, external pacer clock input • General-purpose input bit, target mode
IP1	3	Configurable as one of the following: • TGIN, external trigger or gate input • General-purpose input bit, target mode
IP2	20	Configurable as one of the following: • Counter/timer C/T0 external clock input • General-purpose input bit, target mode
IP3	2	Configurable as one of the following: • Counter/timer C/T1 external clock input • General-purpose input bit, target mode
IP4	19	Configurable as one of the following: • Counter/timer C/T0 external gate input • General-purpose input bit, target mode
IP5	1	Configurable as one of the following: • Counter/timer C/T1 external gate input • General-purpose input bit, target mode

At the multi-functional digital output terminals, three user-selectable options provide three different combinations of available functions. Table 3-15 summarizes specific bit assignments and descriptions for multi-function digital outputs at screw terminals of STP-36, STP-36/C, and STA-3108-A Series accessories.

Table 3-15
Bit assignments and descriptions for multi-function digital outputs

Output mode	Bit assignment	Screw terminal	Description
0	OP0	24	General-purpose output bit, target-mode
	OP1	6	General-purpose output bit, target-mode
	OP2	23	General-purpose output bit, target-mode
	OP3	5	General-purpose output bit, target-mode
	OP4	22	General-purpose output bit, target-mode
	OP5	4	Configurable as one of the following: • TGOUT (trigger-out output) • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output
1	OP0	24	Frame sync
	OP1	6	Counter/timer C/T0 output
	OP2	23	Counter/timer C/T1 output
	OP3	5	Counter/timer C/T2 output
	OP4	22	Pacer-clock output
	OP5	4	Configurable as one of the following: • TGOUT (trigger-out) output • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output
2	OP0	24	External address bit 0 for multiplexing of expansion-accessory channels
	OP1	6	External address bit 1 for multiplexing of expansion-accessory channels
	OP2	23	External address bit 2 for multiplexing of expansion-accessory channels
	OP3	5	External address bit 3 for multiplexing of expansion-accessory channels
	OP4	22	External gain bit for some expansion accessories (e.g. EXP-1800)
	OP5	4	Configurable as one of the following: • TGOUT (trigger-out output) • Pacer clock output • Counter/timer C/T0, CT1, or CT2 output

More information about the configurable functions of the multi-function digital I/O is available as follows:

- The external pacer clock input function (XPCLK) is described in Section 2 in the following sections: "Pacer clock sources," "The external pacer clock (XPCLK) digital input function," and, in context, "Triggers" and "Gates."
- The external trigger or gate input function is described in Section 2 under "Triggers," "Gates," and "The trigger in (TGIN) digital input function." Use of a trigger input signal (TGIN) for multiple-board synchronization is described, in context, in the next section, "Synchronizing multiple boards."
- The trigger output function (TGOUT) is described in Section 2 under "The trigger-out (TGOUT) digital output function" and, in context, in the next section, "Synchronizing multiple boards."
- The pacer clock output is discussed briefly in Section 2 under "The pacer-clock output function."
- Information about the use of address and/or synchronization bits for expansion/signal conditioning-accessories (e.g. for EXP-1800, MB-02) is provided in the instructions that accompany those accessories.
- The nature and use of counter/timer inputs and outputs is discussed in Section 2 under "Counter/timer features" and "The counter/timer digital output functions."
- The nature and use of the multi-function digital I/O for target-mode data transfer is discussed in your DriverLINX documentation.

Wiring counter/timer signals

The multi-function digital I/O bits, after appropriate configuration, are used for all counter/timer inputs and outputs. For information about wiring to these bits, refer to the subsection preceeding, "Wiring multi-function digital I/O signals."

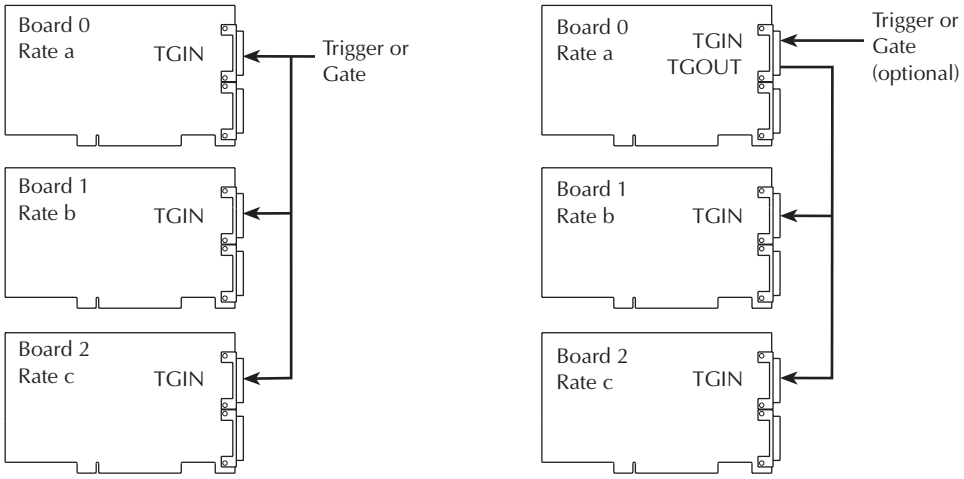
Synchronizing multiple boards

You can synchronize up to three KPCI-3108 boards using trigger and gate signals from the main I/O connectors. A/D (analog-to-digital) conversions at synchronized boards can be started simultaneously by a single event, regardless of whether the boards have been programmed for the same conversion rate or for different conversion rates.

The onboard pacer clock of each board is designed to be tightly coupled with trigger or gate events. Within a short, defined time lag, each synchronized board begins the first analog conversion when the board receives a trigger or gate signal. (Refer to "Triggers" and "Gates" in Section 2). Each board then continues analog conversions at the rate previously set for that board via DriverLINX.

Figure 3-20 shows two connection schemes for synchronizing multiple boards. In both schemes, the conversion rate for each board is timed by the internal pacer clock for that board. When making terminal connections, refer to the preceeding subsection, "Wiring multi-function digital I/O signals."

Figure 3-20
Two connection schemes for synchronizing multiple boards



Board synchronization scheme 1

In Scheme 1, start conversions at synchronized boards with one external trigger/gate signal. Connect the trigger/gate inputs of the boards together such that each board receives the trigger or gate input simultaneously.

A/D conversions at each board start 400 ±100ns after the active edge of a trigger or gate input. Therefore, boards can be synchronized within 100 ±100ns. For example, one board could start conversions as soon as 300ns after the active edge of the trigger input, while another board could start conversions as late as 500ns after the active edge of the trigger input.

When using scheme 1, you can time subsequent A/D conversions using either the onboard pacer clock or an external pacer clock.

Board synchronization scheme 2

In Scheme 2, start conversions in either of two ways: by an external trigger/gate signal or by software. The board connections are in a master/slave relationship; board 0 is the master, and the other boards are the slaves.

If using a hardware trigger for board 0 of scheme 2, board 0 triggers conversions in all boards immediately. Note that TGOUT is an active, high-going signal. Therefore, you must program the TGIN input of each slave board to respond to the positive (rising) edge of the TGOUT signal.

If you use software to enable board 0, the following sequence occurs:

1. The board-0 pacer clock first triggers conversions in the slave boards.
2. Then, conversions start in board 0.

Conversions in board 0 are delayed by a protection feature, which is built into the register that creates software-triggered conversions. This protection feature prevents false conversions.

Wiring +5V power to external circuits

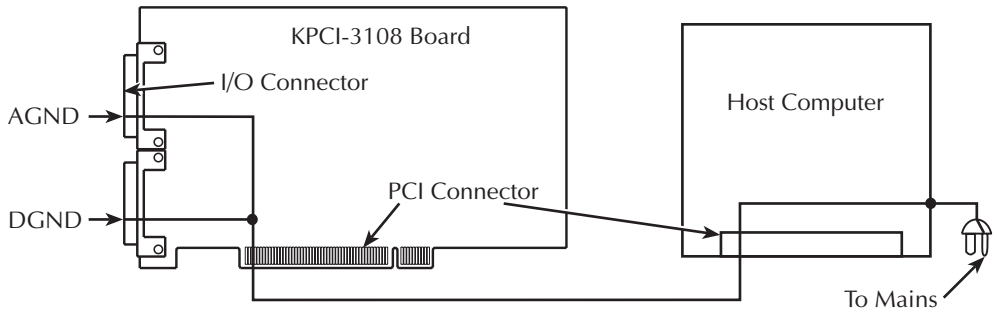
CAUTION **Ensure that both the computer and the external circuit are turned OFF before making any connections. Making connections while the computer and external circuits are powered can damage the computer, the board, and the external circuit.**

Do not connect the +5V output pins to external power supplies. Connecting the +5V output pins to external power supplies may damage the external supplies, the board, and the computer.

Do not draw more than 1.0A, total, from all +5V output pins combined. Drawing more than 1.0A, total, may damage the board. Also, keep in mind that the 5V output comes from the computer power bus. Know the limits of the computer 5V power bus and the current drawn from it by other boards and devices. Other demands on the 5V power bus may limit the current drawn from your board to less than 1.0A.

NOTE *KPCI-3108 boards contain separate ground connections for analog and digital signals. Use the analog ground (AGND) for analog signals and analog power; use the digital ground (DGND) for digital signals and other power-supply returns. Do this to avoid interference from digital switching noise currents on sensitive analog signals. However, be aware that both analog and digital grounds are tied together at the board PCI connector and are ultimately connected to the building system ground via the mains. See Figure 3-21. I/O connector pin assignments and descriptions for AGND and DGND are provided in Figure 3-2, Figure 3-3, Table 3-1, and Table 3-2.*

Figure 3-21
Analog and digital ground path



Power at +5V for light external circuits, such as pull-up resistors, may be drawn indirectly from the host computer power bus via the KPCI-3108 I/O connectors. If you ensure that the following conditions are maintained, this power may also be used to energize external accessories:

- The maximum **total** current drawn from the +5V pins on both I/O connectors combined — pin 25 on the upper "Analog" connector and pins 35 and 36 on the lower "Digital" I/O connector—must be less than 1.0A. The total current drawn to power the board and all external circuits must not overload the computer power bus.
- The total current drawn to power the board and all external circuits must not overload the computer power bus.

Power connections at the upper "Analog" I/O connector and at screw terminals of STP-36, STP-36/C, and STA-3108-A Series accessories connected to it are listed in Table 3-16.

Power connections at the lower "Digital" I/O connector and at screw terminals of STP-36, STP-36/C, and STA-3108-D1 accessories connected to it are listed in Table 3-17.

The +5V power is available at screw terminal accessories as listed.

Table 3-16
Power connections at the upper "Analog" I/O connector

Screw terminal or "Analog" connector pin	Assignment	Description
7	DGND	Digital ground
25	+5 V	+5 VDC from computer bus

Table 3-17
Power connections at the lower "Digital" I/O connector

Screw terminal or "Digital" connector pin	Assignment	Description
17, 18	DGND	Digital grounds
35, 36	+5V	+5 VDC from computer bus

4
DriverLINX Test Panels

The test panels are small applications programs within DriverLINX that allow you to perform limited data acquisition functions. You can use the panels to do tasks such as:

- Monitor one or two analog input channels on-screen.
- Set the levels of one or two analog output channels.
- Monitor and set digital input and output bits.

Test panels are designed primarily for testing the functions of your board. However, one panel in particular — the Analog I/O Panel — can be useful for limited routine tasks.

DriverLINX Analog I/O Panel

The Analog I/O Panel allows you to perform any one of the following five functions at any given time:

- To read voltages from two analog input channels on a digitizing oscilloscope screen. See Figure 4-1.
- To display a DC voltage from one analog input channel on a digital voltmeter screen. See Figure 4-2.
- To send a user-configurable sine-wave, square-wave, or triangular-wave signal from one or two analog output channels (the signal from two channels being identical). See Figure 4-3.
- To control the DC output voltages of two analog output channels. See Figure 4-4.
- To set and read all digital input and output bits on your board. See Figure 4-5.

Figure 4-1
Analog I/O Panel oscilloscope utility

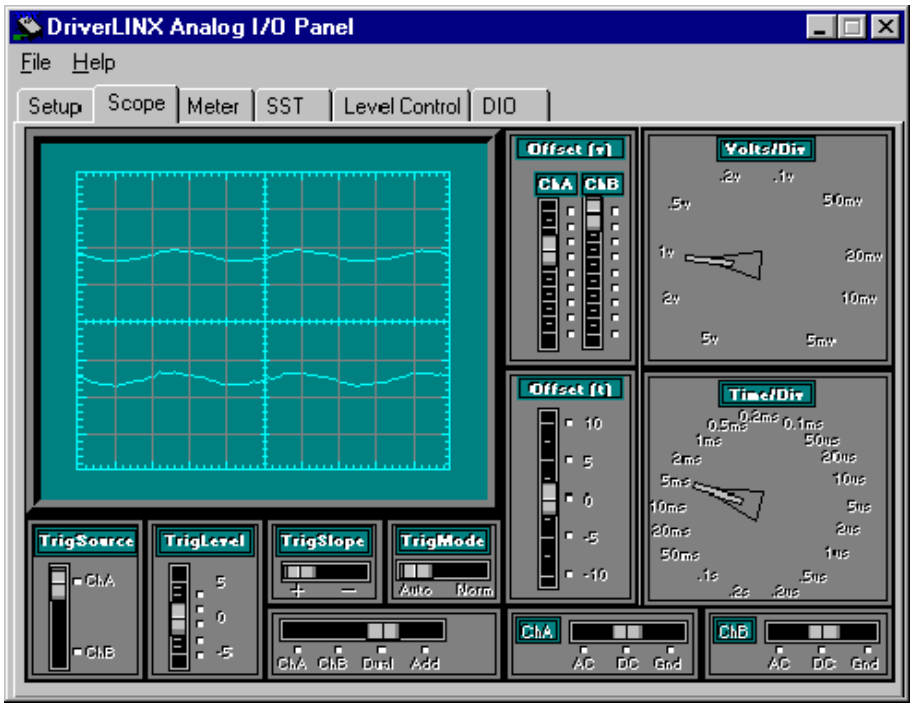


Figure 4-2
Analog I/O Panel digital voltmeter utility

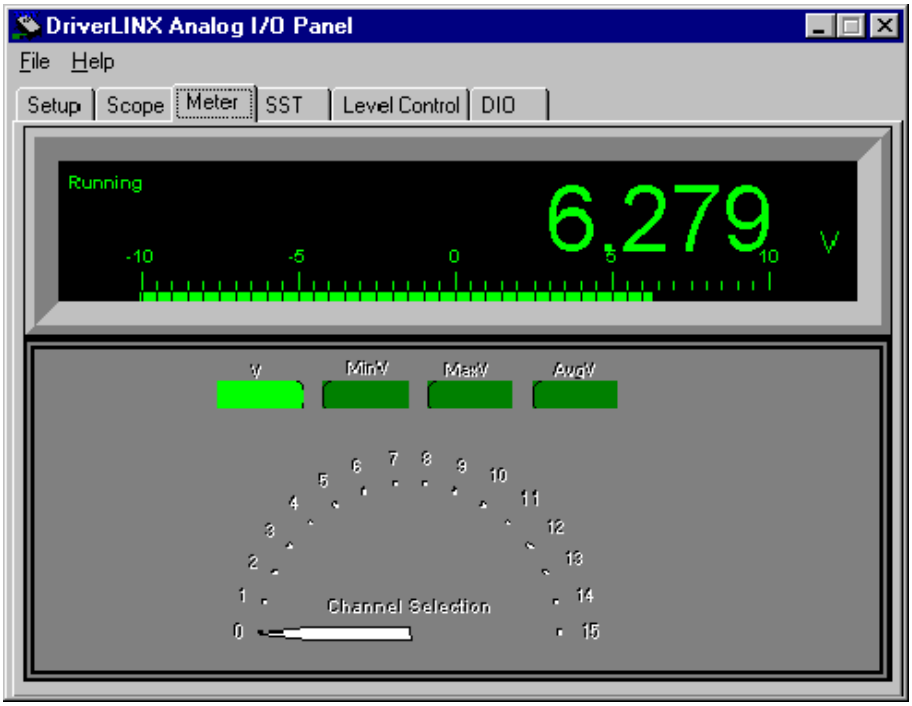

DriverLINX Analog I/O Panel
File Help
Setup Scope Meter SST Level Control DIO
Running
6.279
V
-10 -5 0 5 10
V MinV MaxV AvgV
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Channel Selection

Figure 4-3
Analog I/O Panel function generator utility

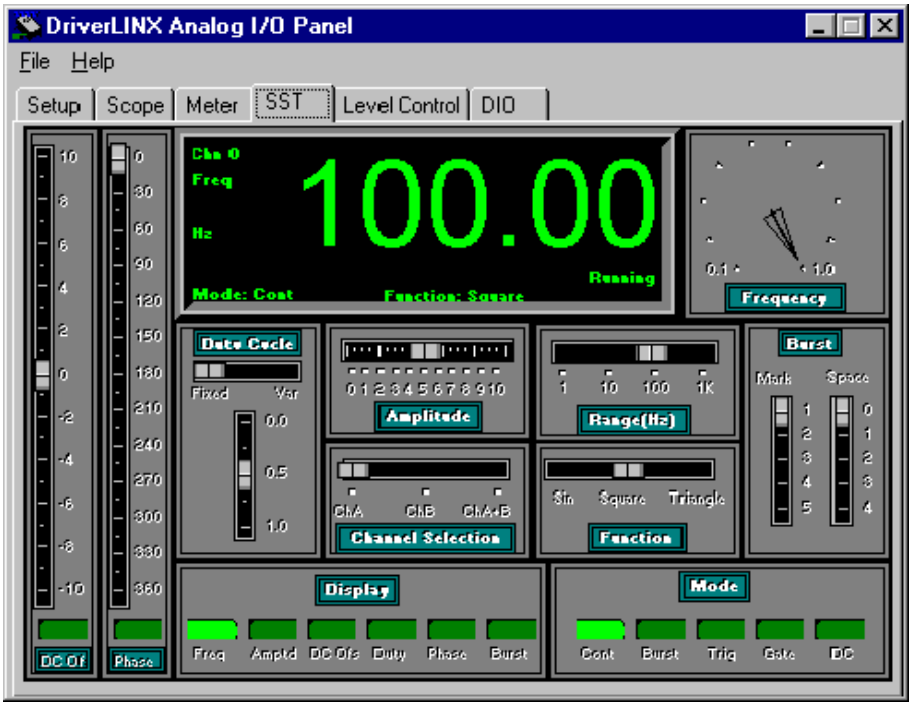


Figure 4-4
Analog I/O Panel output level control utility

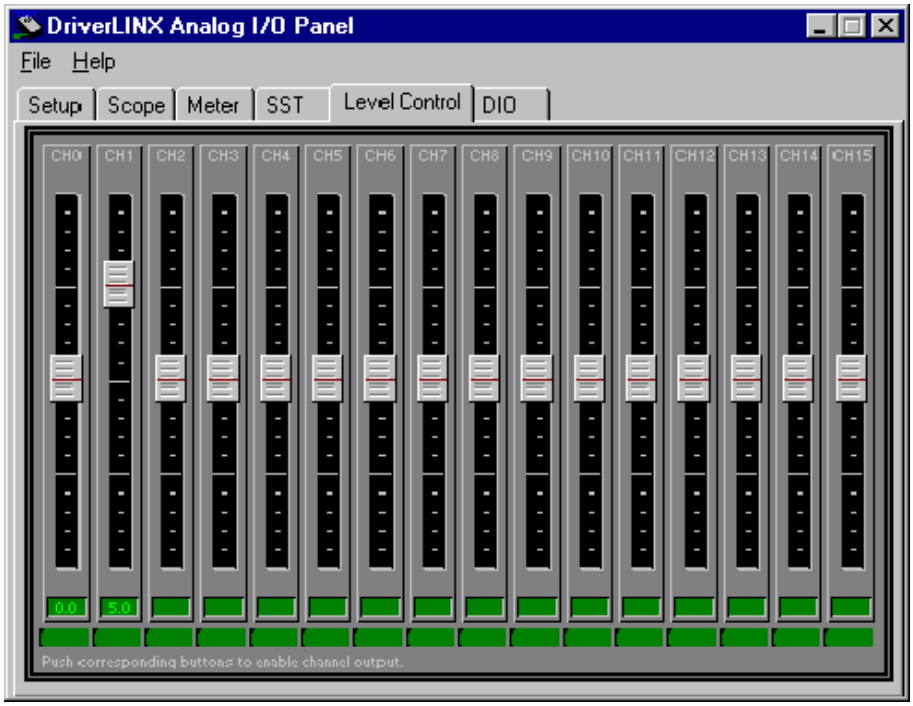
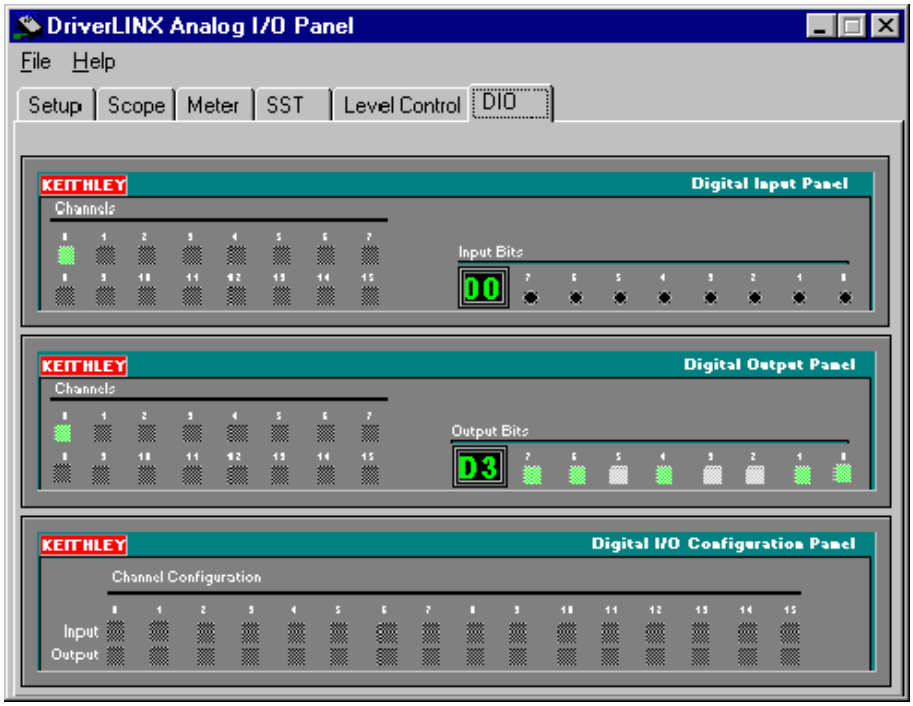

DriverLINX Analog I/O Panel
File Help
Setup Scope Meter SST Level Control DIO
CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CH9 CH10 CH11 CH12 CH13 CH14 CH15
0.0 5.0
Push corresponding buttons to enable channel output.

Figure 4-5
The Analog I/O Panel digital I/O utility

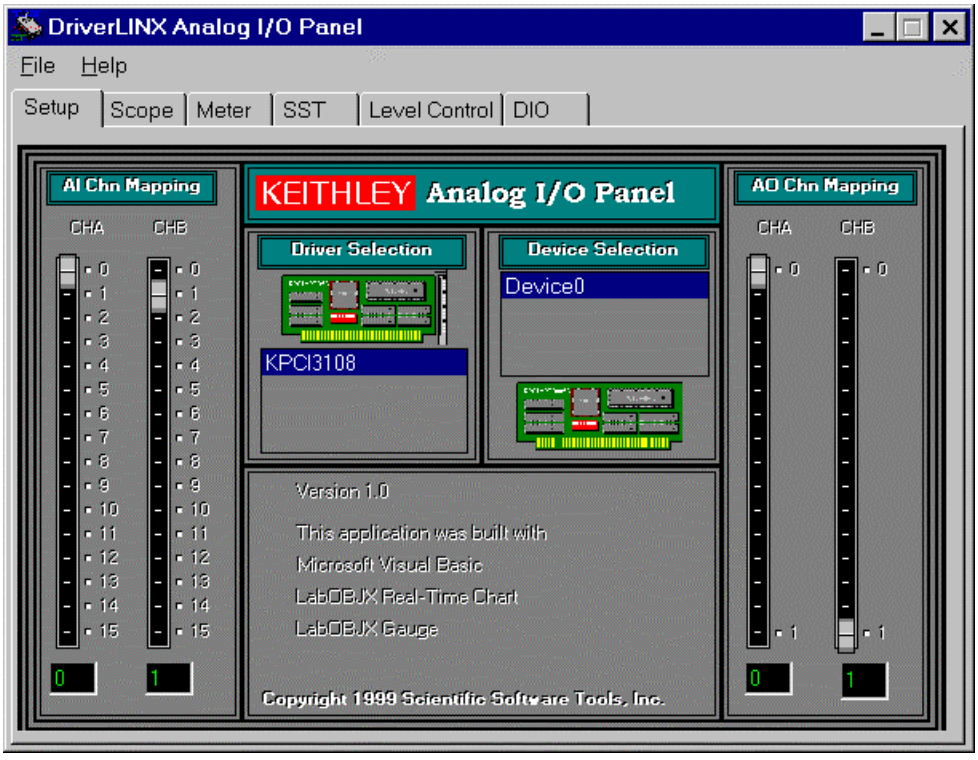


Starting the Analog I/O Panel

Start the DriverLINX Analog I/O Panel as follows:

1. In the **Start** menu, click **Programs.**
2. Find the **DriverLINX** → **Test Panels** folder, under which you should find the **AIO Panel** entry.
3. Click on the **AIO Panel** entry. The Analog I/O Panel setup screen appears.
   - If a KPCI-3108 board is the only board in your computer installed under DriverLINX, only one item appears under Driver Selection. The setup screen looks similar to Figure 4-6.
   - If more than one type of board is installed in your computer under DriverLINX, the Analog I/O Panel may appear similar to Figure 4-6, but with multiple drivers listed under **Driver Selection** and multiple devices listed under **Device Selection** (for example, **Device0, Device1**, etc.).Your board type and device number may not be displayed initially, and fewer tabs may be displayed at the top of the screen than in Figure 4-6. If so, click the scroll buttons next to the Driver Selection and Device Selection text boxes until your KPCI-3108 board type and device number are displayed. All six tabs will then be displayed.

Figure 4-6
Analog I/O Panel setup screen similar to the screen that appears when only a KPCI-3108 board is installed under DriverLINX



Using the Analog I/O panel

For more details about the program, refer to the Analog I/O Panel help menu. To review test procedures that use the digital voltmeter and level control utilities of the AIO panel, refer to "Analog input hardware test" and "Analog output hardware test" in Section 6. For a procedure using the digital I/O utility of the AIO panel, refer to "General-purpose digital I/O hardware test" in Section 6.

DriverLINX Calibration Utility

The DriverLINX Calibration Utility automates many of the operations required to calibrate the analog I/O of your board. This is possible because the KPCI-3108 board does not have calibration potentiometers. Instead, it is 100% digitally calibrated, using on-board trimming digital-to-analog converters (trim DACs). On-screen instructions lead you through the operations that you must perform.

For more information about the DriverLINX Calibration Utility, refer to Section 5, "Calibration."

5
Calibration

Introduction

Your KPCI-3108 board was initially calibrated at the factory. You are advised to check the calibration of a board every six months and to calibrate again when necessary. This chapter provides the information you need to calibrate a KPCI-3108 board.

Objectives

For analog inputs, the objective of this procedure is to zero the offsets and adjust the combined gain of the A/D converter and instrumentation amplifier. For analog outputs, the objective is to independently zero the offset and adjust the gain for each of the two digital-to-analog converters (DACs) on your KPCI-3108 board.

Calibration summary

Analog inputs and outputs are calibrated using a DC calibrator, a DVM/DMM, and the DriverLINX Calibration Utility. (The DriverLINX Calibration Utility was installed on your computer when you installed the DriverLINX software.) No calibration potentiometers must be adjusted. Instead, on-board trimming digital-to-analog converters (trim DACs) are adjusted digitally through the Calibration Utility software. No test points on the board are used. Only connections to the I/O connector pins, via a screw terminal accessory, are needed.

Each of the twelve unipolar and twelve bipolar analog input ranges is individually calibrated. For each range, three eight-bit trim-DAC values are searched for and then adjusted: a gain value, a coarse-offset value, and a fine-offset value. Therefore, a complete analog input calibration involves 72 adjustments: 2 polarities x 12 gains/polarity x 3 adjustments/gain.

For a KPCI-3108 analog output, each of the two unipolar and two bipolar output ranges is individually calibrated. For each range, two eight-bit trim-DAC values are searched for and then adjusted: a gain value and an offset value. Therefore, a complete calibration of both analog outputs involves 16 adjustments: 2 polarities x 2 gains/polarity x 2 adjustments/gain x 2 analog outputs.

The trim DAC calibration values are stored in on-board nonvolatile RAM (NVRAM), which retains its contents even when the board is unpowered. During bootup (only), DriverLINX reads these values and stores them in on-board CalRAM, from which they are fetched as needed in real time.

Equipment

The following equipment is needed to calibrate your KPCI-3108 board:

- A digital voltmeter (DVM) or digital multimeter (DMM) accurate to 6-½ digits, such as a Keithley Model 2000.
- An STP-36 or STP-36/C screw terminal accessory to make analog connections to the board.
- A Keithley CAB-1284CC Series cable or a standard IEEE 1284 Type C-C mini-Centronics cable to connect the screw terminal accessory to the upper "Analog" I/O connector of the KPCI-3108 board.
- A DC calibrator or precisely adjustable and metered power supply having up to a 10VDC range and accurate to 6-½ digits.

Calibration procedure (preliminary)

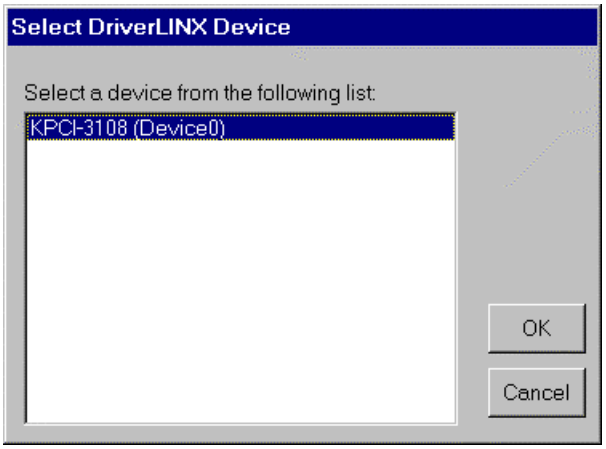
This section describes the steps required to calibrate the analog inputs and outputs of your KPCI-3108 board.

Preparing for the calibrations

Prepare your system for calibration as follows:

1. Warm up the calibrator and the DVM/DMM.
2. Turn OFF the host computer.
3. Connect the STP-36 or STP-36/C screw terminal accessory to your KPCI-3108 board, using the CAB-1284CC Series or equivalent cable. Refer to Section 3, "Connecting interface accessories to a KPCI-3108 board" for more information about connecting these accessories.
4. Turn ON the host computer.
5. Start the calibration utility as follows:
   a. Click on the Windows **Start** tab.
   b. In the **Start** menu, click **Programs**.
   c. Find the **DriverLINX** folder and click the **Test Panels** → **KPCI-3108 Calibration Utility** entry. The Select DriverLINX Device dialog box appears, similar to Figure 5-1.

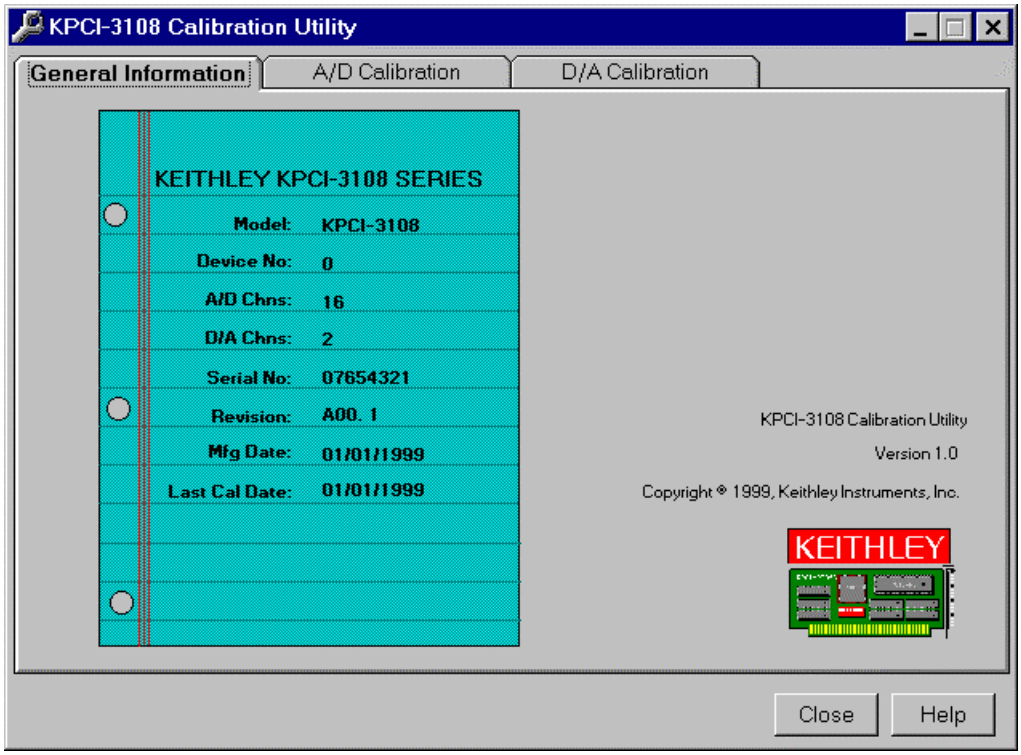
Figure 5-1
The Select DriverLINX Device dialog box



d. In the Select DriverLINX Device dialog box, select your board and click **OK**. The KPCI-3108 Calibration Utility dialog box appears, similar to Figure 5-2.

e. Continue with the next section, "Calibrating the analog inputs."

Figure 5-2
KPCI-3108 calibration utility

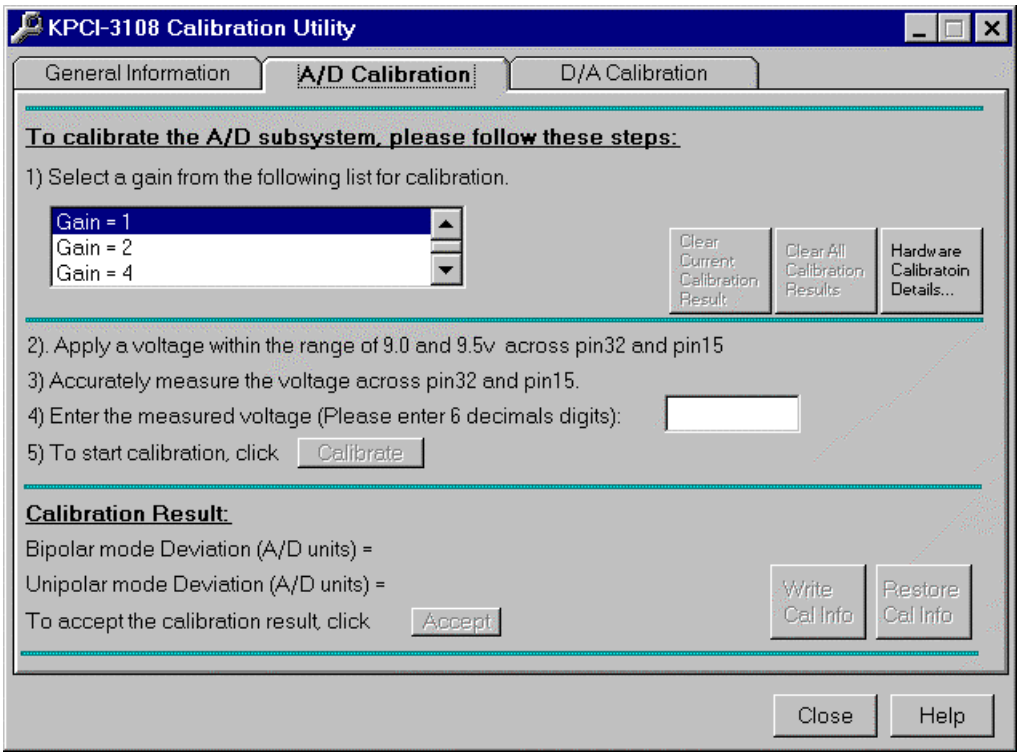


Calibrating the analog inputs

In this part of the procedure, offset and gain adjustments for the analog input and A/D Converter (ADC) circuits are made. Do the following:

1. In the KPCI-3108 Calibration Utility dialog box, click the **A/D Calibration** tab. The A/D Calibration dialog box appears. See Figure 5-3.
2. To calibrate the analog inputs, follow the on-screen instructions in the A/D Calibration dialog box.
3. When finished with the analog input calibration, continue with the next section, "Calibrating the analog outputs."

Figure 5-3
A/D calibration dialog box

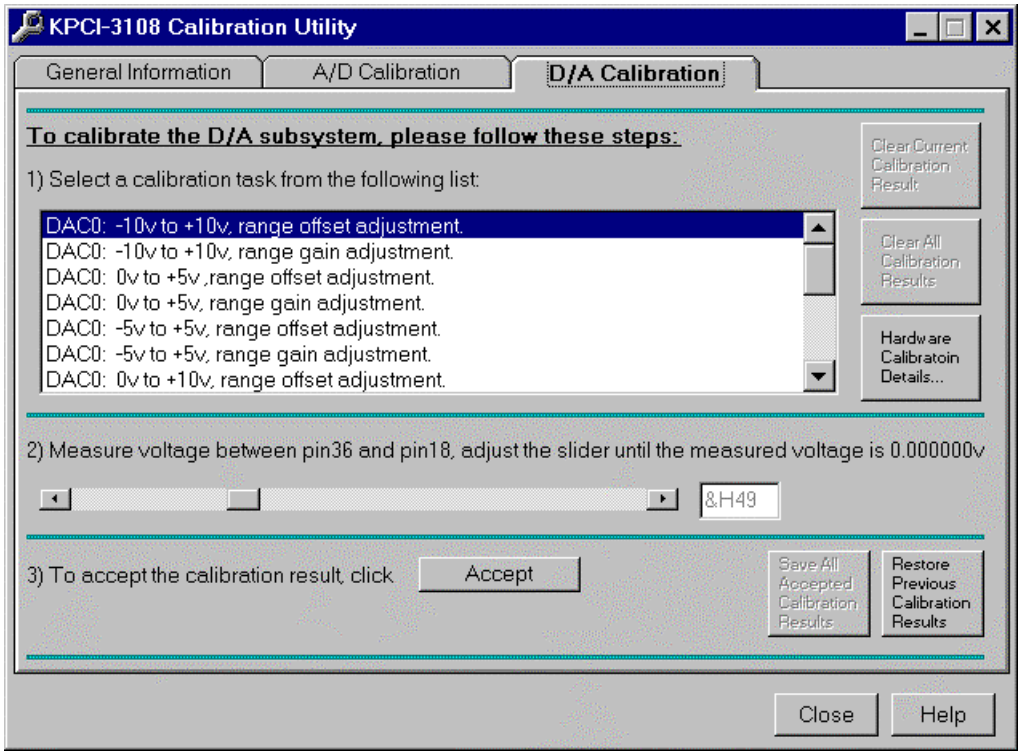

KPCI-3108 Calibration Utility
General Information
A/D Calibration
D/A Calibration
To calibrate the A/D subsystem, please follow these steps:
1) Select a gain from the following list for calibration.
Gain = 1
Gain = 2
Gain = 4
Clear Current Calibration Result
Clear All Calibration Results
Hardware Calibratoin Details...
2). Apply a voltage within the range of 9.0 and 9.5v across pin32 and pin15
3) Accurately measure the voltage across pin32 and pin15.
4) Enter the measured voltage (Please enter 6 decimals digits):
5) To start calibration, click
Calibrate
Calibration Result:
Bipolar mode Deviation (A/D units) =
Unipolar mode Deviation (A/D units) =
To accept the calibration result, click
Accept
Write Cal Info
Restore Cal Info
Close
Help

Calibrating the analog outputs

The KPCI-3108 boards each have two independent analog outputs, provided by two digital-to-analog converters (DACs or D/A converters). In this part of the procedure, offset and gain adjustments for the DACs are made. Do the following:

1. In the KPCI-3108 Calibration Utility dialog box, click the **D/A Calibration** tab. The D/A Calibration dialog box appears. See Figure 5-4.
2. To calibrate each DAC, follow the on-screen instructions in the D/A Calibration dialog box.

Figure 5-4
D/A Calibration dialog box


KPCI-3108 Calibration Utility
General Information
A/D Calibration
D/A Calibration
To calibrate the D/A subsystem, please follow these steps:
1) Select a calibration task from the following list:
DAC0: -10v to +10v, range offset adjustment.
DAC0: -10v to +10v, range gain adjustment.
DAC0: 0v to +5v ,range offset adjustment.
DAC0: 0v to +5v, range gain adjustment.
DAC0: -5v to +5v, range offset adjustment.
DAC0: -5v to +5v, range gain adjustment.
DAC0: 0v to +10v, range offset adjustment.
Clear Current Calibration Result
Clear All Calibration Results
Hardware Calibratoin Details...
2) Measure voltage between pin36 and pin18, adjust the slider until the measured voltage is 0.000000v
&H49
3) To accept the calibration result, click
Accept
Save All Accepted Calibration Results
Restore Previous Calibration Results
Close
Help

6
Troubleshooting

This chapter provides the following two approaches to troubleshooting:

- A list of general symptoms and possible solutions under "Identifying symptoms and possible causes."
- A series of detailed, systematic troubleshooting schemes and associated procedures under "Systematic problem isolation."

If your KPCI-3108 board is not operating properly, use the information in this chapter to isolate the problem before calling Keithley Applications Engineering. If, after completing the troubleshooting procedures, you still need to contact an applications engineer, refer to the "Technical support" section.

Identifying symptoms and possible causes

You may be able to isolate the problem using Table 6-1, which lists general symptoms and possible solutions for KPCI-3108 board problems.

Table 6-1
Basic troubleshooting information

Symptom	Possible cause	Possible cause validation/solution
Computer does not boot when board is installed.	Resource conflict. KPCI-3108 board is conflicting with other boards in the system.	1. Validate the cause of the conflict. Temporarily unplug boards — especially ISA boards[1] — one at a time, and try booting the computer. Repeat until a boot is attained. 2. Try resolving conflicts by reinstalling one PCI board at a time and rebooting after each reinstallation.[2] However, you may ultimately need to change ISA board resource allocations, such as base address or interrupt assignments.
	Board not seated properly.	Check the installation of the board.
	The power supply of the host computer is too small to handle all the system resources.	Check the needs of all system resources and obtain a larger power supply.
After board and software are installed, mouse control is lost or system freezes.	An interrupt conflict occurred.	Unplug the board to regain mouse control. Look closely at the COM ports and at the interrupts of other devices.
Board does not respond to the Analog I/O Panel that comes with the KPCI-3108 DriverLINX.	DriverLINX is not installed properly.	Check the Windows Device Manager and follow the installation troubleshooting instructions in the DriverLINX on-line help.
	The board is incorrectly aligned in the expansion slot.	Check the board for proper seating.
	The board is damaged.	Contact Keithley Applications Engineering.

Table 6-1 (cont.)
Basic troubleshooting information

Symptom	Possible cause	Possible cause validation/solution
Data appears to be invalid.	An open connection exists.	Check screw terminal wiring.
	Transducer is not connected to channel being read.	Check the transducer connections.
	Signal and/or connections inappropriate for the selected input mode, differential or single-ended.	Ensure that correct input mode — differential or single-ended — is being used for your signal conditions and that input is wired properly for this mode. Refer to Section 3, "Wiring analog input signals."
Intermittent operation	Vibrations or loose connections exist.	Cushion source of vibration and tighten connections.
	The board is overheating.	Check environmental and ambient temperature. Refer to your computer documentation.
	Electrical noise exists.	Provide better shielding or reroute unshielded wiring.
System lockup during operation.	A timing error occurred.	Restart your computer. Then analyze your program by debugging and narrowing the list of possible failure locations.

[1]Plug and Play cannot tell if an ISA board already uses an address that it assigns to a PCI board.
[2]Plug and Play may then assign different, nonconflicting addresses to the PCI boards.

If your board is not operating properly after using the information in Table 6-1, continue with the next section to further isolate the problem.

Systematic problem isolation

If you were unable to isolate the problem by using Table 6-1, then try to isolate the problem systematically using the schemes detailed in this section.

For clarity, the systematic problem isolation procedure is divided into seven schemes, each of which checks for, eliminates, and/or resolves problem causes. Each scheme consists of a flowchart and, in most cases, an amplified written procedure. The numbers of flowchart blocks are keyed to the numbers of written steps.

For simplicity, your problem is assumed to have only one cause. One particular scheme may not alone isolate this cause. Rather, performance of several schemes in series may be required to analyze your problem. One scheme may eliminate potential causes from further consideration, then direct you to another scheme(s) that ultimately isolates the problem. You need perform only those schemes to which you are directed.

If the cause of your problem appears to be outside the scope of the systematic isolation procedure, the procedure directs you to call Keithley for help.

The seven problem isolation schemes are as follows:

- Scheme A checks for three basic system problems.
- Scheme B checks DriverLINX installation and board recognition by DriverLINX.
- Scheme C addresses application software issues.
- Scheme D addresses apparent expansion slot malfunctions and attempted remedies.
- Scheme E addresses potential external connection problems.
- Scheme F addresses apparently malfunctioning board(s).
- Scheme G verifies that earlier schemes have found and addressed the problem.

Start the systematic isolation procedure at the next section, entitled "Problem isolation Scheme A: basic system," unless you have been directed otherwise in this manual. (The board/DriverLINX installation check in Section 3 of this manual sends you directly to Scheme B.)

CAUTION **Always turn OFF your computer and any external circuits connected to the KPCI-3108 board before removing or replacing the board. Removing or replacing a board with the power ON can damage the board, the computer, the external circuit, or all three.**

Handle the board at the mounting bracket, using a grounded wrist strap. Do not touch the circuit traces or connector contacts.

NOTE *In the following procedure, the term "board" always refers to a KPCI-3108 board. The procedure never directs you to install or remove any type of board other than a KPCI-3108 board.*

In the flowcharts of Schemes A through G, the number in brackets in each block (e.g. [6]) refers to the corresponding step number in the amplified written procedure. If multiple blocks in the flowchart have the same number, each of those blocks is part of a single verbal step. Conversely, if there is a range of numbers in the brackets (e.g. [4, 5 or 8-10], the block summarizes multiple verbal steps.

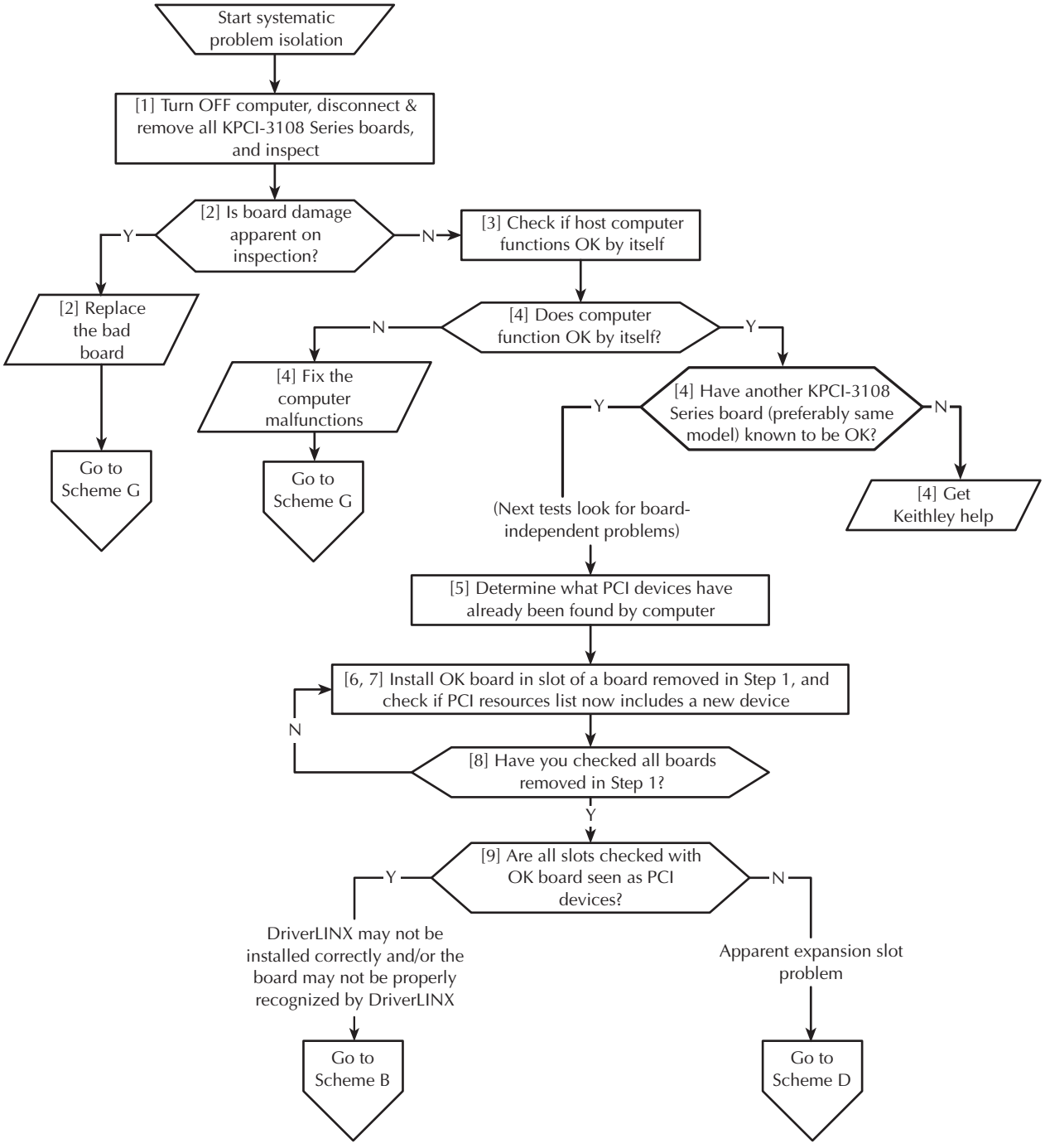
The logic used in the systematic problem isolation schemes assumes that the problem has only one cause. Therefore, once a cause is found and corrected, the reader is instructed to reassemble the system and verify proper operation.

Each individual scheme in this procedure, except for Scheme A, is designed to be used only if called for by other schemes or procedures. For example, Scheme B is called for by Scheme A. Scheme B is also called for as a post-installation check in Section 3 of this manual and in the "Read This First" sheet that shipped with your board. If you attempt to use schemes independently, you lose the benefits of systematic problem isolation.

Problem isolation Scheme A: basic system

In Scheme A, you start the systematic problem isolation procedure. You remove your KPCI-3108 board(s) and check for apparent damage. If the board looks okay, you check the independent functionality of your computer. If the computer is okay, you check the expansion slots that held your KPCI-3108 board(s). Refer to Figure 6-1 and the written amplification following it.

Figure 6-1
Problem isolation Scheme A: basic system


Start systematic problem isolation
[1] Turn OFF computer, disconnect & remove all KPCI-3108 Series boards, and inspect
[2] Is board damage apparent on inspection?
Y
N
[2] Replace the bad board
Go to Scheme G
[3] Check if host computer functions OK by itself
[4] Does computer function OK by itself?
N
Y
[4] Fix the computer malfunctions
Go to Scheme G
[4] Have another KPCI-3108 Series board (preferably same model) known to be OK?
Y
N
[4] Get Keithley help
(Next tests look for board-independent problems)
[5] Determine what PCI devices have already been found by computer
[6, 7] Install OK board in slot of a board removed in Step 1, and check if PCI resources list now includes a new device
N
[8] Have you checked all boards removed in Step 1?
Y
[9] Are all slots checked with OK board seen as PCI devices?
Y
N
DriverLINX may not be installed correctly and/or the board may not be properly recognized by DriverLINX
Go to Scheme B
Apparent expansion slot problem
Go to Scheme D

Follow these amplified instructions as you perform Scheme A:

1. Remove and inspect the KPCI-3108 board(s) for damage as follows:
   a. Shut down Windows 95/98/NT and turn OFF power to the host computer.
   b. Turn OFF power to all external circuits and accessories connected to the KPCI-3108 board(s) that is installed.

c. Disconnect STP-36 or STP-36/C screw terminal accessories from your KPCI-3108 board(s).

d. Remove the KPCI-3108 boards from the computer, making note of the socket(s) in which the board(s) was installed. (If more than one KPCI-3108 board is installed, remove all boards and note which board was in which socket.)

e. Visually inspect all removed KPCI-3108 board(s) for damage.

2. Based on the results of 1, do the following:

- If the board(s) you removed in step 1 is obviously damaged, then repair or replace the board. Refer to "Technical support" for information on returning the board for repair or replacement. Skip to "Problem isolation Scheme G: verification of problem solution."
- If the board(s) you removed in step 1 is not obviously damaged, then continue with step 3 and check for host computer malfunction.

3. Check if the computer functions satisfactorily by itself. Proceed as follows:

a. Place the board(s) that you removed from the computer in step 1 in an electrostatically safe location. Do not reinstall it.

b. Turn ON power to the host computer.

c. Perform all needed diagnostics to determine whether your computer hardware and operating system are functioning properly.

4. Based on the results of step 3, do one of the following:

- If you find no computer or operating system malfunctions in step 3, then the problem likely lies elsewhere; take action as follows:
  - If you do not have another KPCI-3108 board that you know is good, i.e. works properly, read the instructions in "Technical support." Then contact Keithley for help in isolating the cause of your problem.
  - If you have another KPCI-3108 board that you know is good, i.e. works properly, then continue with step 5.

    Preferably, the good KPCI-3108 board should have the same model number as the board(s) that was removed. Alternatively, a different KPCI-3108 board that minimally has all the features of the board(s) that was removed is satisfactory. (For example, a KPCI-3108 board substitutes for a KPCI-3107 board. The KPCI-3108 has all the features of the KPCI-3107, plus analog outputs not available in the KPCI-3107). Using the same model, or a features-plus model, of good KPCI-3108 board is not so important in Scheme A. However, it is important in other schemes that follow Scheme A. Those other schemes assume that the correct model of good board was previously installed in Scheme A.
- If you find computer or operating system malfunctions in step 3, do the following:
  a. Determine the cause of the computer hardware or operating system malfunctions.
  b. Fix the computer hardware or operating system malfunctions.
  c. Assume that fixing the malfunctions has solved your problem, and skip to "Problem isolation Scheme G: verification of problem solution."

5. Determine the PCI resources detected by your computer before any KPCI-3108 boards are installed. Proceed as follows:

a. Shut down Windows 95/98/NT and turn OFF power to the host computer.

b. Insert a blank diskette, or any diskette that you are sure is unbootable, into the A: drive.

c. Turn ON the computer and allow it to start the boot cycle.

The boot cycle stalls at a text screen listing system characteristics and resources and saying at the bottom: **Non-system disk or disk error. Replace and press any key when ready.**

NOTE *This system characteristics and resources screen is normally displayed only fleetingly during the boot cycle. Having an unbootable diskette in your computer automatically stops the boot cycle at this screen, allowing for convenient viewing. This is not harmful to your computer. The more common approach — using the* PAUSE *key to pause the boot cycle at this screen — requires fast reflexes with some systems.*

d. Note the displayed list of PCI devices under a heading something like **PCI device listing…** If you have a printer, print the screen by pressing the PRINT SCREEN key.

e. Remove the diskette and allow the boot cycle to finish.

6. Install a good board — a KPCI-3108 board that you know is fully functional — as follows:

   a. Shut down Windows 95/98/NT and turn OFF power to the host computer.

   b. Install the good board in the slot from which you removed the potentially faulty board in step 1. Refer to "Installing the KPCI-3108 board" near the beginning of Section 3, for board installation instructions.

NOTE *If you removed more than one board in step 1, install only one good board in only one expansion slot.*

Do not connect any external circuits to the board at this point.

7. Again determine the PCI resources detected by your computer, after the KPCI-3108 board is installed. Windows 95 Plug and Play should find and configure the new board as a PCI resource if all of the following are true:

   - The board functions properly as a PCI device.
   - The contacts of the expansion slot in which the OK board is installed are in good condition.
   - The OK board is seated properly in the expansion slot.

   Do the following, as you did in step 5:

   a. Insert an unbootable diskette.

   b. Turn ON the computer and allow the boot cycle to stall at the **Non-system disk or disk error…** message.

   c. Again, note the displayed list of PCI devices. A new device should be listed, likely as an unidentified peripheral. If your resource listing includes PCI slot numbers, the slot number for the new device should match the number of the slot in which your board is installed.

   d. Remove the diskette and allow the boot cycle to finish.

8. If you removed KPCI-3108 boards from other PCI slots in step 1, then repeat steps 6 and 7 with the good board in each of these other slots.

9. Based on the results of steps 5 through 8, do one of the following:

   a. If the good board is recognized as a PCI component in all slots tested, then the PCI slots are apparently satisfactory. DriverLINX may not be installed correctly and/or the board may not be properly configured. Continue with "Problem isolation Scheme B: installation."

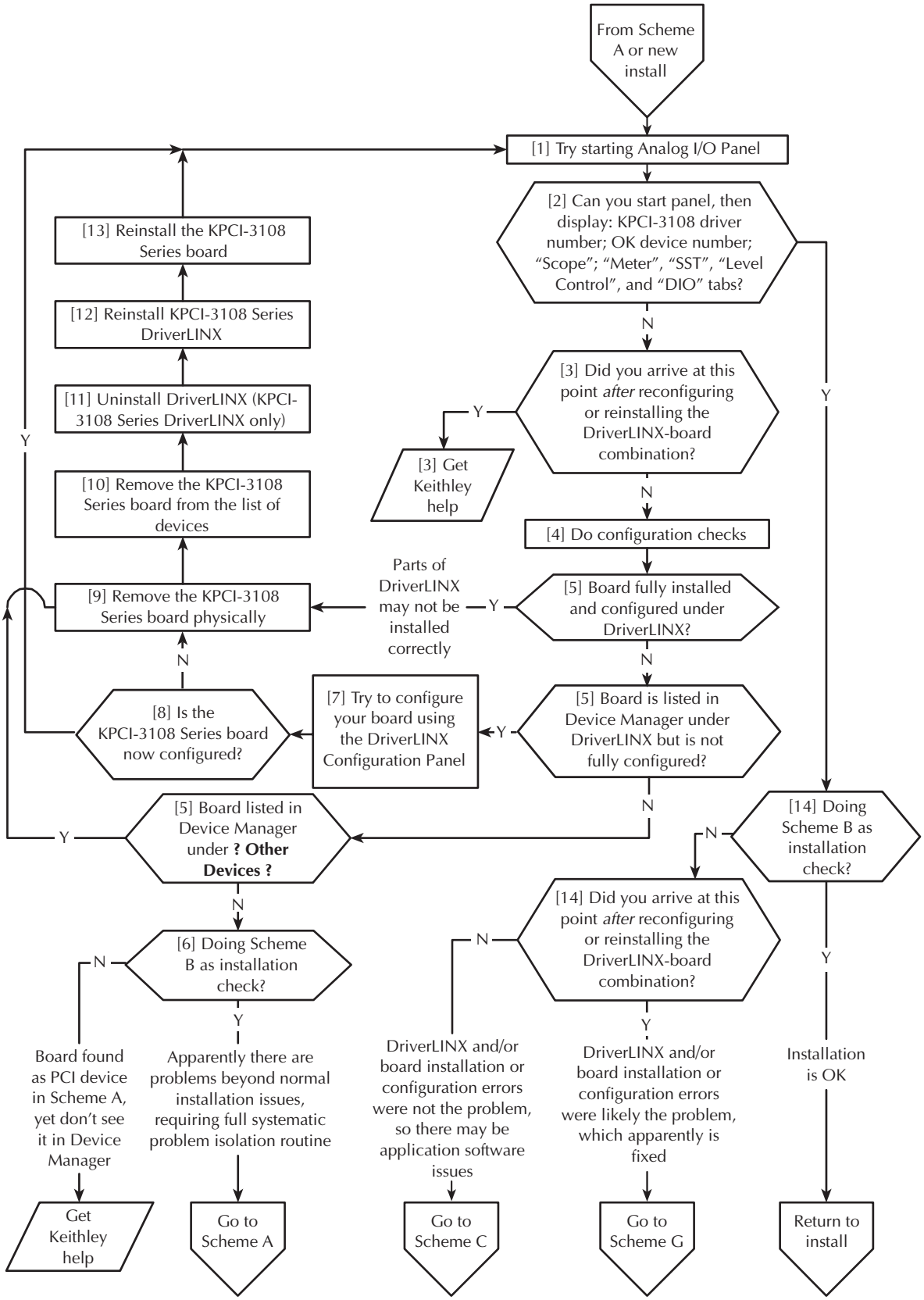
   b. If the good board is not recognized as a PCI component in a slot(s), then the PCI slot connector(s) is suspect. Continue with "Problem isolation Scheme D: expansion slot connectors."

Problem isolation Scheme B: installation

In Scheme B, you check whether DriverLINX and your board are installed correctly and work together properly. A proper start of the DriverLINX Analog I/O Panel utility means that the combined DriverLINX/board installation is okay. If the installation is not okay, you try to diagnose and fix the problem, ultimately reinstalling DriverLINX and the board if necessary. Refer to Figure 6-2 and the written amplification following it.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

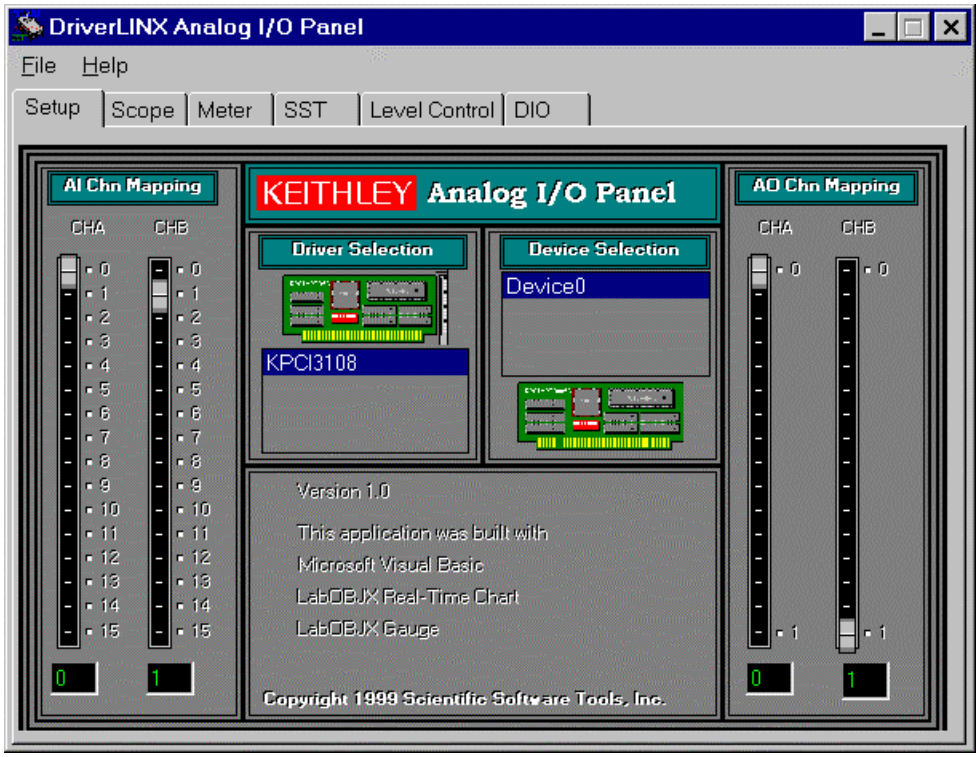
Figure 6-2
Problem isolation Scheme B: installation


From Scheme A or new install
[1] Try starting Analog I/O Panel
[2] Can you start panel, then display: KPCI-3108 driver number; OK device number; "Scope"; "Meter", "SST", "Level Control", and "DIO" tabs?
N
Y
[3] Did you arrive at this point *after* reconfiguring or reinstalling the DriverLINX-board combination?
Y
[3] Get Keithley help
N
[4] Do configuration checks
[5] Board fully installed and configured under DriverLINX?
Parts of DriverLINX may not be installed correctly
Y
N
[5] Board is listed in Device Manager under DriverLINX but is not fully configured?
Y
[7] Try to configure your board using the DriverLINX Configuration Panel
[8] Is the KPCI-3108 Series board now configured?
N
[9] Remove the KPCI-3108 Series board physically
[10] Remove the KPCI-3108 Series board from the list of devices
[11] Uninstall DriverLINX (KPCI-3108 Series DriverLINX only)
[12] Reinstall KPCI-3108 Series DriverLINX
[13] Reinstall the KPCI-3108 Series board
Y
N
[5] Board listed in Device Manager under **? Other Devices ?**
Y
N
[6] Doing Scheme B as installation check?
N
Y
Board found as PCI device in Scheme A, yet don't see it in Device Manager
Get Keithley help
Apparently there are problems beyond normal installation issues, requiring full systematic problem isolation routine
Go to Scheme A
[14] Doing Scheme B as installation check?
N
Y
[14] Did you arrive at this point *after* reconfiguring or reinstalling the DriverLINX-board combination?
N
Y
DriverLINX and/or board installation or configuration errors were not the problem, so there may be application software issues
Go to Scheme C
DriverLINX and/or board installation or configuration errors were likely the problem, which apparently is fixed
Go to Scheme G
Installation is OK
Return to install

Follow these amplified instructions as you perform Scheme B:

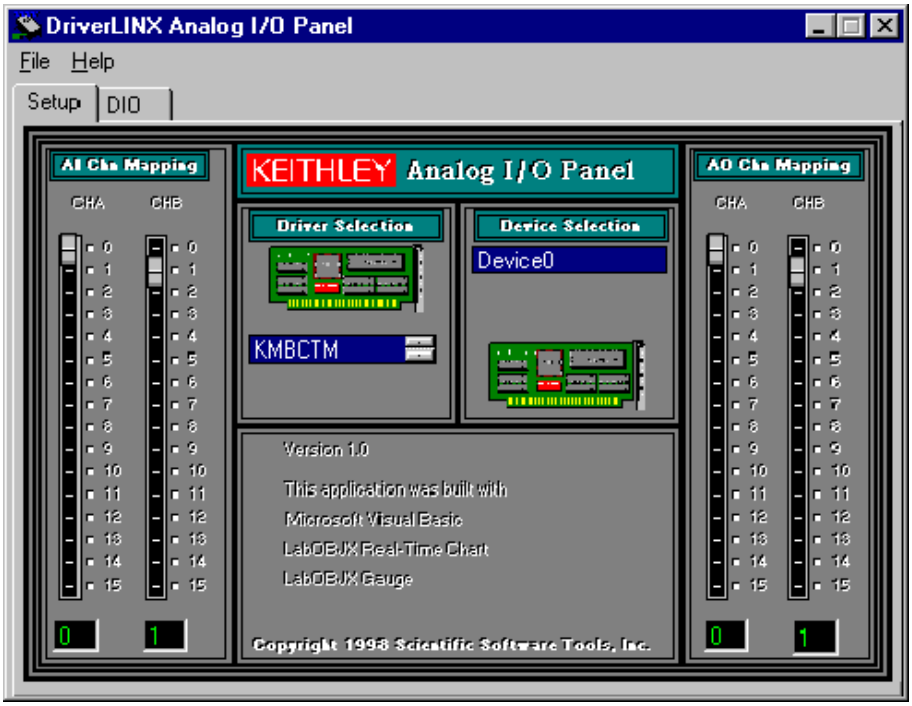
1. Try starting the DriverLINX Analog I/O Panel. Proceed as follows:
   a. In the **Start** menu, click **Programs.**
   b. Find the **DriverLINX** → **Test Panels** folder, under which you should find the **AIO Panel** entry.
   c. Click on the **AIO Panel** entry.
2. Based on the results of Step 1, select one of the following:
   - Case A — If both of the following statements are true, then skip to step 14; DriverLINX and your board are installed properly and are working together.
     – A KPCI-3108 board is the only board in your computer installed under DriverLINX.
     – The DriverLINX Analog I/O Panel appears similar to Figure 6-3, with **KPCI3108** listed under **Driver Selection.**

Figure 6-3
Analog I/O Panel setup screen example with only KPCI-3108 boards installed



- Case B — If all three of the following statements are true, then skip to step 14; DriverLINX and your board are installed properly and are working together.
  - More than one type of board is installed in your computer under DriverLINX.
  - The DriverLINX Analog I/O Panel initially appears similar to Figure 6-3, but perhaps more similar to Figure 6-4 with any or all of the following differences: 1) tiny buttons located at the right side of the **Driver Selection** text box and/or the **Device Selection** text box; 2) a different board driver under **Driver Selection**; 3) a different device number under **Device Selection**; 4) different tabs at the top of the screen. See Figure 6-4.
  - The tabs at the top of the screen look like the tabs in Figure 6-3 after you do the following, using the tiny buttons next to the text boxes: 1) select the board driver under **Driver Selection** to be **KPCI3108** and 2) select the correct device number under **Device Selection**, which is **0** if only one KPCI-3108 board is installed.

Figure 6-4
Analog I/O Panel example setup screen with multiple board types installed



- Case C — If neither of the two scenarios above apply — neither Case A nor Case B, then continue with step 3; there may be a problem with the DriverLINX installation and/or the board configuration.

3. Select the next step in Scheme B based on the criteria given in the following alternatives:
   - If you have already reconfigured or reinstalled DriverLINX and the board, yet still cannot successfully start the Analog I/O Panel, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support" and then contact Keithley for help in isolating the cause of your problem.
   - If you have not yet tried to fix the combined DriverLINX/board problem, then continue with step 4.
4. See if and how your KPCI-3108 board is listed in the Windows Device Manager. Proceed as follows:

a. Right-click the **My Computer** icon on your desktop.

b. On the menu that appears, click **Properties**.

c. On the System Properties dialog box that appears, click the **Device Manager** tab. The Device Manager appears.

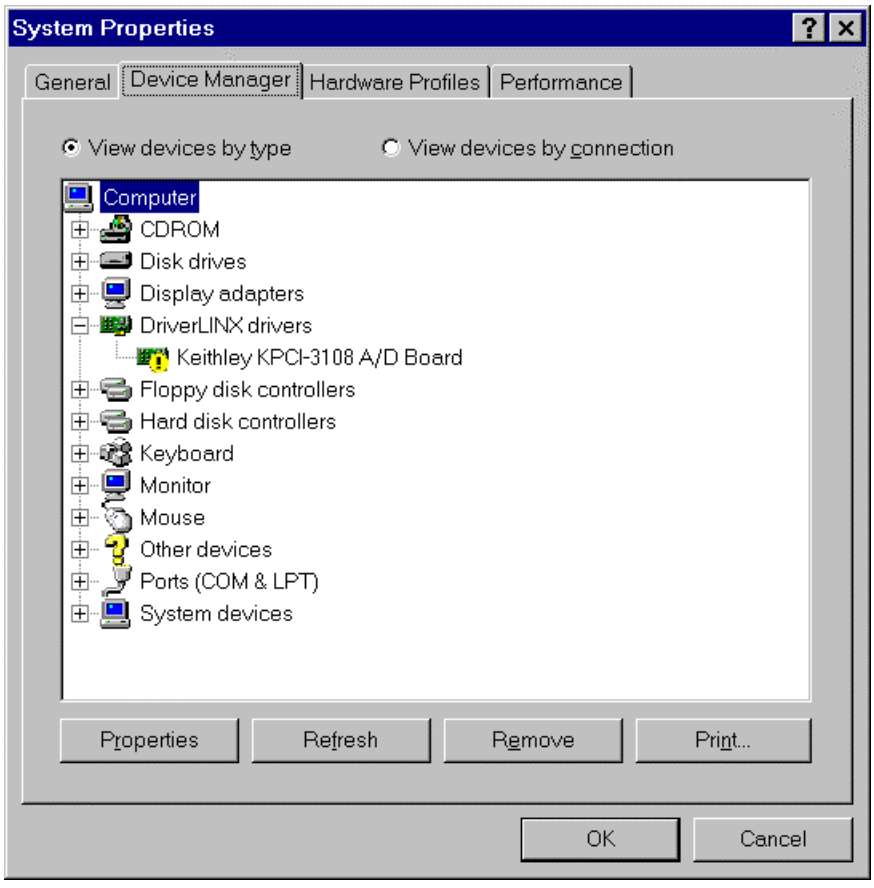
d. In the Device Manager look for a **DriverLINX drivers** item.

e. If you find a **DriverLINX drivers** item, click the + sign to the left of this item. A second level list may appear with the specific model number of your KPCI-3108 board. More than one KPCI-3108 board may be listed here if you installed more than one KPCI-3108 board.

f. Select your next action based on the criteria given in the following alternatives:

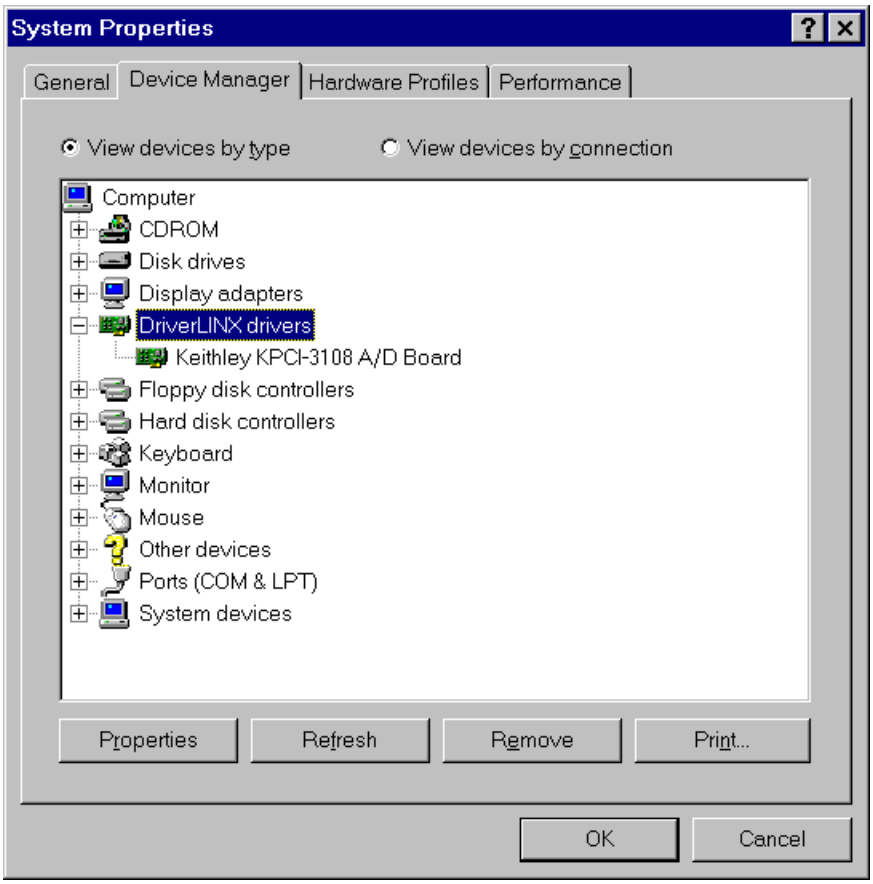
- If a board is recognized as a device under DriverLINX but is not configured to work with DriverLINX, then the board is normally listed with a large exclamation point over it, as shown in Figure 6-5. If you find a KPCI-3108 board listed with an exclamation point over it, keep the Device Manager open and go directly to step 5. Skip substeps 4g through 4j.

Figure 6-5
Listing of improperly configured/installed KPCI-3108 board



- If a board is recognized as a device under DriverLINX and *is* configured to work with DriverLINX, then the board is listed without the large exclamation point over it, as shown in Figure 6-6. However, though a listing as in Figure 6-6 is a necessary indication of a complete KPCI-3108 board configuration, it is not by itself a sufficient indication in at least one situation. Therefore, if you find that *all* of your KPCI-3108 boards are listed in the Device Manager without exclamation points, do as follows:
  1) Leave the Device Manager open for now.
  2) Continue with substeps 4g through 4j, in which you open and check the DriverLINX Configuration Panel.

Figure 6-6
Appearance of device manager listing when KPCI-3108 board is properly configured/installed



- If the list of devices in the Device Manager includes an **? Other Devices** item, also click the + sign to the left of this item (see the **?** near the bottom of Figure 6-6). If a KPCI-3108 board is listed under **? Other Devices**, then keep the Device Manager open and go directly to step 5. Skip substeps 4g through 4j.
- If one or more of your KPCI-3108 boards is not listed anywhere in the Device Manager, then keep the Device Manager open and go directly to step 5. Skip substeps 4g through 4j.

g. In the **Start** menu, click **Programs.**

h. Find the **DriverLINX** folder and under it click **DriverLINX Configuration Panel.** The DriverLINX Configuration Panel appears. See the examples in Figure 6-7 and Figure 6-8.

Figure 6-7
Example of a DriverLINX Configuration Panel before a KPCI-3108 board is configured

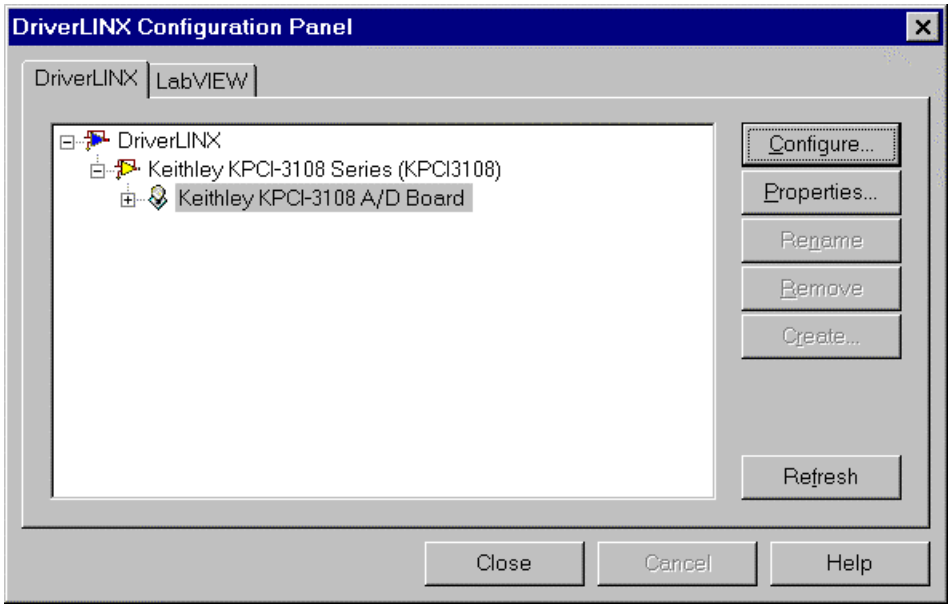
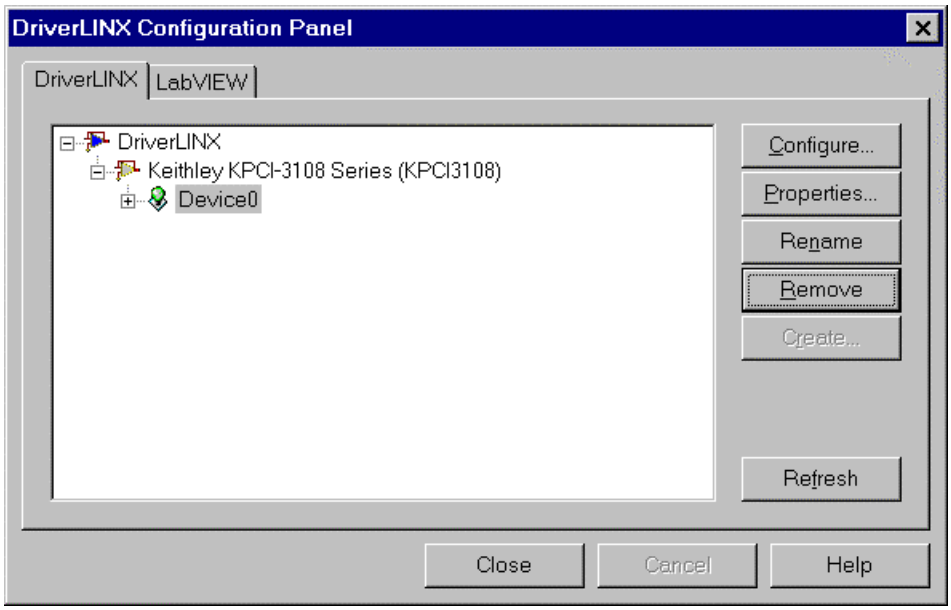


Figure 6-8
Example of a DriverLINX Configuration Panel after a KPCI-3108 board is configured



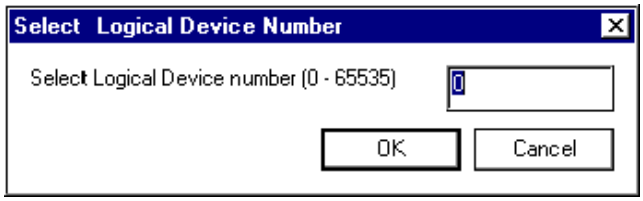
i. Inspect the DriverLINX Configuration Panel.
   - If you see the following on the screen for a KPCI-3108 board, illustrated in Figure 6-7, then the board is recognized as a device under DriverLINX but is not properly configured:
     – **Keithley KPCI-3108 Series** is listed under DriverLINX.
     – The amplifier icon next to **Keithley KPCI-3108 Series** is colored yellow.
     – The specific board part number(s) of the unconfigured Keithley KPCI-3108 board(s) is listed under Keithley KPCI-3108.
     – The lamp icon next to the specific board part number is uncolored.
   - If you see the following on the screen for a KPCI-3108 board, illustrated in Figure 6-8, then the board is recognized as a device under DriverLINX and *is* properly configured:
     – **Keithley KPCI-3108 Series** is listed under DriverLINX.
     – The amplifier icon next to **Keithley KPCI-3108 Series** is colored pale gray.
     – A device number — for example, **Device0** (or **Device1, Device2,** etc.**)**— is listed under **Keithley KPCI-3108 Series**, instead of a specific board part number.
     – The lamp icon next to the device number is colored green.

j. Leave the DriverLINX Configuration Panel open for now and continue with step 5.

5. Based on the results of step 4, do one of the following:
   - If your board is properly installed and configured, your inability to run the Analog I/O Panel may be due to an improperly installed component of DriverLINX. Skip to step 9, and begin uninstalling, then reinstalling DriverLINX and the board.
   - If one of your KPCI-3108 boards is apparently recognized by DriverLINX but is listed in the Device Manager under DriverLINX with a large exclamation point, then try configuring it with the DriverLINX Configuration Panel. Skip to step 7.
   - If one of your KPCI-3108 boards is listed under **? Other Devices**, or is listed in the Device Manager at multiple places, then the installation is faulty. Skip to step 9 and begin uninstalling, then reinstalling DriverLINX and the board.
   - If your board is not listed at all in the Device Manager, there are apparently issues other than the combined DriverLINX/board installation. Continue with step 6.
6. Select the next step in Scheme B based on the criteria given in the following alternatives:
   - If you are performing Scheme B independently as an installation check, then non-installation issues must apparently be resolved before you can successfully run your board. Starting at "Problem isolation Scheme A: basic system," proceed through the systematic problem isolation procedure.
   - If you are performing Scheme B as part of the systematic problem isolation procedure, then you should have seen your board listed in the device manager at this point in the procedure. The cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.
7. Try to reconfigure your board using the DriverLINX configuration panel, which you opened in step 4 and should still be open. Proceed as follows:
   a. In the DriverLINX Configuration Panel, select an unconfigured KPCI-3108 board by clicking on its part number. An unconfigured KPCI-3108 board may be identified as follows:
      - The specific board part number of the unconfigured Keithley KPCI-3108 board is listed under **Keithley KPCI-3108 Series**.
      - The lamp icon next to the specific board part number is uncolored.
      - The amplifier icon next to **Keithley KPCI-3108 Series** is colored yellow.

b. Click the **Configure** button. The Select Logical Device dialog box appears as in Figure 6-9.

Figure 6-9
Selecting the logical device number



c. Select your next action based on the criteria given in the following alternatives:

- If only one KPCI-3108 board is installed, a default device number of **0** in the text box is correct. Click **OK**.
- If other KPCI-3108 boards are installed and configured and have been assigned device numbers, then type in a device number for the board you are configuring — the next, unassigned number in the numbering sequence. Then click **OK**.

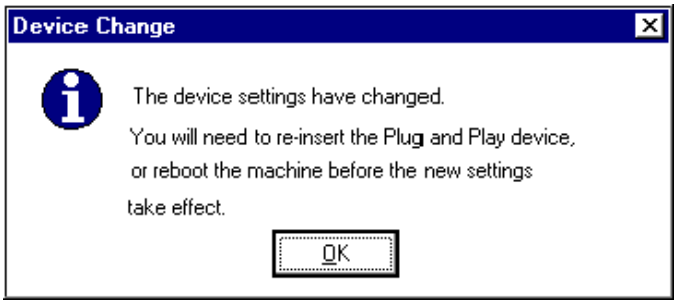
The Configure DriverLINX Device dialog box appears, Figure 6-10, as well as the Device Manager.

Figure 6-10
Configure DriverLINX Device dialog box example

d. No changes in the Device dialog box are normally required. Click **OK**.

e. If a Device Change message appears as in Figure 6-11, then click **OK**.

Figure 6-11
Device Change message


Device Change
The device settings have changed.
You will need to re-insert the Plug and Play device,
or reboot the machine before the new settings
take effect.
OK

f. If more than one unconfigured board was found in the DriverLINX Configuration Manager in step 4, configure the additional boards now. Repeat substeps 7a through 7e for each remaining unconfigured board.

g. Close out all programs and reboot your computer to complete the configuration process.

h. Open and check the Device Manager as you did in step 4. Your KPCI-3108 board(s) should now be listed under the DriverLINX with no exclamation mark over it, as was illustrated in Figure 6-6.

i. Open and check the DriverLINX Configuration panel as you did in step 4. If you successfully configured your board(s), you should now see the following listed below **Keithley KPCI-3108 Series**. Refer back to step 4i and Figure 6-8.

- Instead of a specific board part number(s), there should now be a device number(s) — for example, **Device0**.
- The lamp icon next to the device number(s) should be colored green.

8. Based on the results of step 7, do one of the following:
   - If the board was successfully configured, return to step 1 and retry starting the Analog I/O Panel.
   - If the board was not successfully configured, continue with step 9 and begin uninstalling, then reinstalling DriverLINX and the board.
9. Remove all KPCI-3108 boards physically.

NOTE *You should remove all KPCI-3108 boards before reinstalling the KPCI-3108 version of DriverLINX, because the installation order is DriverLINX first, board second. If a KPCI-3108 board is present, physically or in the computer list of devices, driver installation difficulties may occur.*

Proceed as follows:

a. Turn OFF the computer.

b. Remove all KPCI-3108 boards from their computer expansion slots.

CAUTION **Wear a grounded wrist strap to avoid electrostatic damage to the board. Do not touch board components or conductors when handling the board.**

10. Remove all KPCI-3108 boards from the list of devices in your system. If your operating system is Windows 95/98, remove the KPCI-3108 boards using the Windows 95/98 Device Manager, as follows:
    a. Shut down and turn OFF the computer.
    b. Open the Device Manager by right clicking the **My Computer** icon, clicking **Properties** on the menu that appears, then clicking the **Device Manager** tab. A list of installed devices appears. See example in Figure 6-5.
    c. Select your next step based on the criteria given in the following alternatives:
       - If the Device Manager lists a **DriverLINX drivers** item, click the **+** sign to the left of this item. A second level list may appear with the specific model number of your KPCI-3108 board. More than one KPCI-3108 board may be listed if you previously installed more than one KPCI-3108 board. Alternatively, if a previously installed board is not properly recognized by DriverLINX, it may not be listed here or may be listed with a large exclamation point over it.
       - If the Device Manager lists an **? Other Devices** item, also click the **+** sign to the left of this item. You should not, but could, find a KPCI-3108 board listed under this item if it is not properly recognized by DriverLINX.
    d. Select any one of the KPCI-3108 boards that you find in the Device Manager, wherever you find it.
    e. At the bottom of the list of devices, click **Remove**.
    f. On the Confirm Device Removal dialog box that appears, click **OK**. The board is removed from the list of devices.
    g. If more than one KPCI-3108 board was listed in the Device Manager, or if the same board was listed in more than one place, then repeat substeps d, e, and f of step 10 until no KPCI-3108 boards are listed anywhere in the Device Manager.
11. Uninstall *only* the KPCI-3108 version of DriverLINX from your system using the Windows 95/98/NT Add/Remove Programs feature. Proceed as follows:
    a. In the **Start** menu of Windows 95/98/NT, click **Settings → Control Panel.**
    b. In the Control Panel that appears, click **Add/Remove Programs.**
    c. In the Add/Remove Programs Properties dialog box that appears, select **DriverLINX for Keithley 3108**.

NOTE *Uninstall only* **DriverLINX for Keithley 3108**. *If additional DriverLINX versions are installed, leave them installed.*

    d. At the bottom of the Add/Remove Programs Properties dialog box, click **Add/Remove** and then follow the remainder of the Windows uninstall prompts.

CAUTION **During the course of an uninstall procedure, you will typically be asked if you wish to uninstall certain files that may be shared by other programs. In such cases, always click *No*. Mistakenly uninstalling files needed by other programs causes serious problems. Mistakenly keeping files causes no harm, and some uninstalled files may be overwritten anyway when you subsequently reinstall DriverLINX.**

12. Reinstall DriverLINX, referring to the brief DriverLINX installation instructions on the Read This First sheet that was shipped with your KPCI-3108 board and is also provided on the CD-ROM containing this manual. Make sure that DriverLINX installs smoothly and completely.
13. Reinstall the board(s).

CAUTION **Wear a grounded wrist strap to avoid electrostatic damage to the board. Do not touch board components or conductors when handling the board.**

NOTE *If you are performing Scheme B independently as an installation check, then reinstall all boards that you removed in step 9. If you are performing Scheme B as part of the systematic problem isolation procedure, then reinstall only the good board that you began using near the end of Scheme A.*

Proceed as follows:

a. Shut down and turn OFF the computer.
b. Install the board(s) in its expansion slot(s), following this brief procedure in Section 3 of the manual: "Installing the KPCI-3108 board."
c. Turn ON and reboot the computer.
d. Run the procedure in Section 3, "Configuring the board to work with DriverLINX."
e. Return to step 1 and run the installation check again.

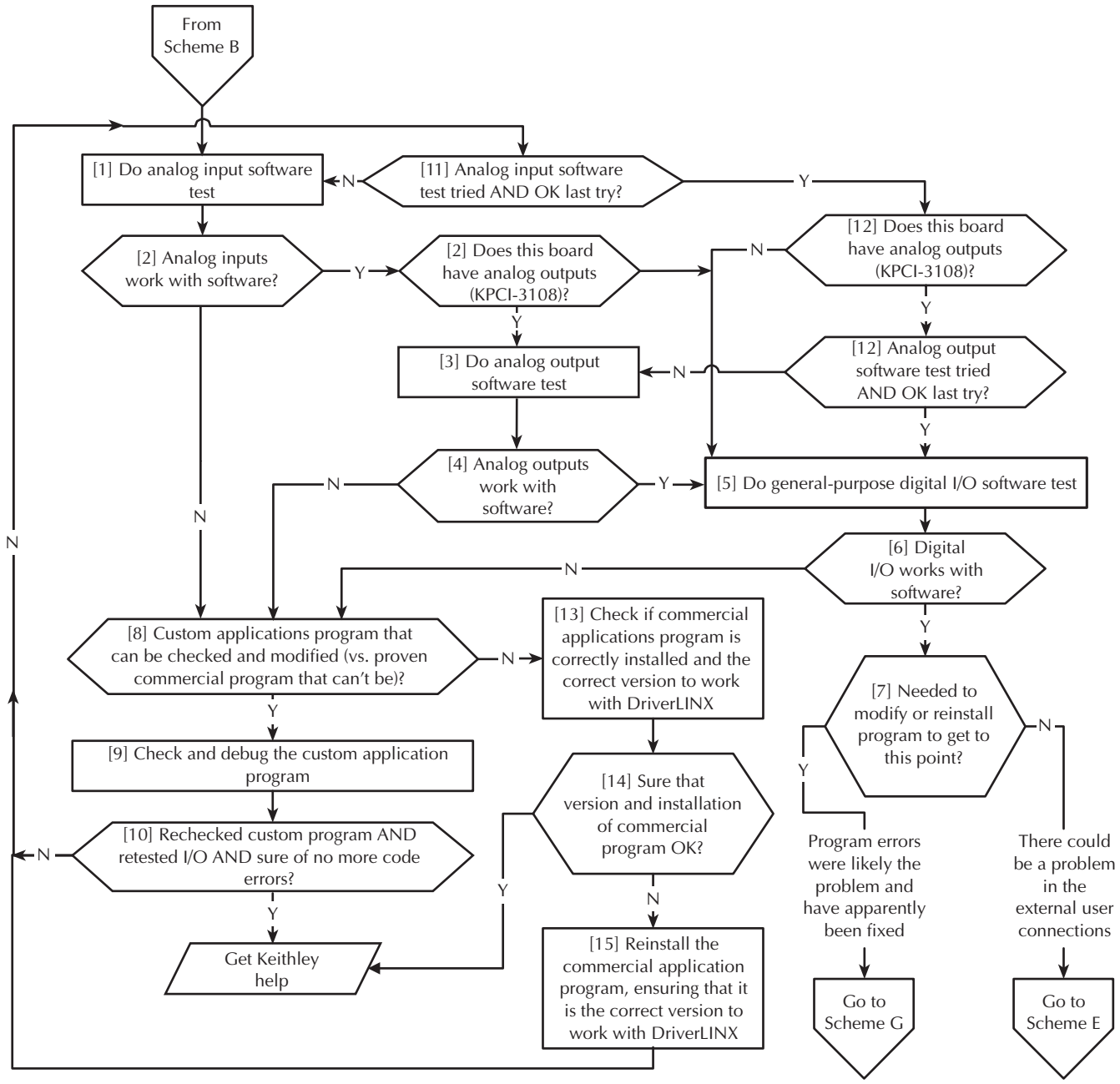
14. You arrived at this step from step 2, after successfully starting the Analog I/O Panel. Select your next action based on the criteria given in the following alternatives:
    - If you are performing Scheme B independently as an installation check, then DriverLINX and your KPCI-3108 board are installed correctly. Return to Section 3 and finish installing your data acquisition system, starting with "Identifying I/O connector pin assignments for KPCI-3108."
    - If you performed Scheme B as part of the systematic problem isolation procedure AND arrived at this point after reconfiguring the board or reinstalling DriverLINX and the board, then that effort with "Problem isolation Scheme G: verification of problem solution."
    - If you performed Scheme B as part of the systematic problem isolation procedure AND arrived at this point without performing any remedial efforts, then your problem must lie elsewhere. Go to "Problem isolation Scheme C: application software" and check for application software issues.

Problem isolation Scheme C: application software

In Scheme C, you check for bugs in custom application software, assuming that you can access the source code. Alternatively, you check for compatibility and installation issues in commercial application software. In Scheme A, you temporarily installed a KPCI-3108 board that is known to be good in place of a KPCI-3108 board that you removed from the computer. This substitution, still in place, eliminates possible board I/O problems during Scheme C. You now perform I/O tests using your application software. You debug custom code, if necessary, and recheck. Refer to Figure 6-12 and the written amplification following it.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

Figure 6-12
Problem isolation Scheme C: application software


From Scheme B
[1] Do analog input software test
[11] Analog input software test tried AND OK last try?
N
Y
[2] Analog inputs work with software?
Y
[2] Does this board have analog outputs (KPCI-3108)?
N
[12] Does this board have analog outputs (KPCI-3108)?
Y
[3] Do analog output software test
N
[12] Analog output software test tried AND OK last try?
Y
[4] Analog outputs work with software?
N
Y
[5] Do general-purpose digital I/O software test
N
[6] Digital I/O works with software?
N
Y
[8] Custom applications program that can be checked and modified (vs. proven commercial program that can't be)?
N
[13] Check if commercial applications program is correctly installed and the correct version to work with DriverLINX
Y
[9] Check and debug the custom application program
[7] Needed to modify or reinstall program to get to this point?
N
Y
[10] Rechecked custom program AND retested I/O AND sure of no more code errors?
N
[14] Sure that version and installation of commercial program OK?
Y
N
Y
Get Keithley help
[15] Reinstall the commercial application program, ensuring that it is the correct version to work with DriverLINX
Program errors were likely the problem and have apparently been fixed
There could be a problem in the external user connections
Go to Scheme G
Go to Scheme E

Follow these amplified instructions as you perform Scheme C:

1. Perform the procedure outlined in the "Analog input software test," found later in Section 6.
2. Based on the results of the Analog input software test, do one of the following:
   - If your software appears not to be working properly with your analog inputs, skip to step 8.
   - If your software appears to be working properly AND your board does *not* have analog outputs (for example, a KPCI-3107 board), skip to step 5.
   - If your software appears to be working properly AND your board has analog outputs (for example, a KPCI-3108 board), continue with step 3.
3. Perform the procedure outlined in the "Analog output software test" found later in Section 6.
4. Based on the results of the Analog output software test, do one of the following:
   - If your software appears not to be working properly with your analog outputs, skip to step 8.
   - If your software appears to be working properly with your analog outputs, continue with step 5.
5. Perform the procedure outlined in the "General-purpose digital I/O software test" found later in Section 6.
6. Based on the results of the "General-purpose digital I/O software test", do one of the following:
   - If your software appears not to be working properly with your digital I/O, skip to step 8.
   - If your software appears to be working properly with your digital I/O, continue with step 7.
7. Select the next step in Scheme C based on the criteria given in the following alternatives:
   - If you reached this point without modifying the custom software or reinstalling the commercial software—if you experienced no problems in the tests at any point—then the problem you originally experienced must lie elsewhere. Go to "Problem isolation Scheme E: user wiring" and check your external connections.
   - If you reached this point by having to modify the custom software or reinstall the commercial software—if you no longer experience problems in the tests—then assume that you have solved the original problem. Go to "Problem isolation Scheme G: verification of problem solution" and verify that the problem is solved.
8. You arrived at this point because one of the I/O software tests failed. Select the next step in Scheme C based on the criteria given in the following alternatives:
   - If your applications program is a proven program—potentially a commercial program that you cannot modify—then the software may be installed incorrectly or perhaps is incompatible with DriverLINX. Skip to step 13.
   - If your applications program is a custom program that can be modified—the source code is available—then continue with step 9.
9. Check and debug the source code as necessary.

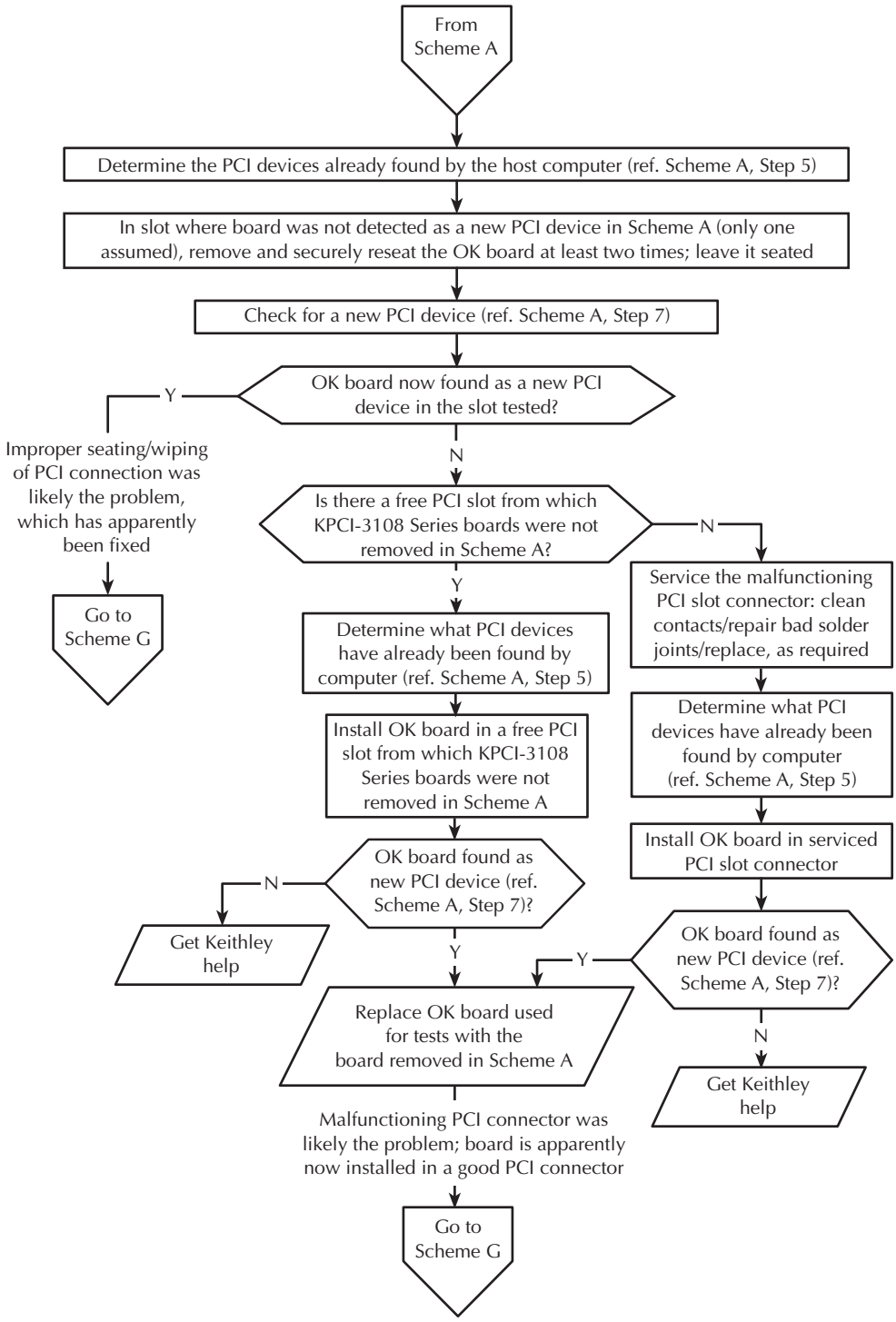
10. At this point, you have presumably found and corrected some program bugs. Select the next step in Scheme C based on the criteria given in the following alternatives:
    - If *both* of the following statements are true, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.
      – You are at this point after having debugged the source code at least once and after having failed the I/O software tests at least a second time.
      – You have tried to find more code bugs after two or more I/O test failures and cannot find any more bugs.
    - If none or only one of the above statements are true, then continue with step 11, and selectively redo I/O software tests.
11. Select your next step in Scheme C based on the criteria given in the following alternatives:
    - If you have done the analog input software test at least once AND your software did not pass the analog input software test the last time, then return to step 1 and redo that test.
    - If you have done the analog input software test at least once AND your software passed the analog input software test the last time, then assume that you do not need to repeat it. Continue with step 12.
12. Select your next step in Scheme C based on the criteria given in the following alternatives:
    - If all three of the following apply, then return to step 3 and redo the analog output software test:
      – Your board has analog outputs (for example, you have a KPCI-3108 board).
      – You have done the analog output software test at least once.
      – Your software did not pass the analog output software test the last time you tried.
    - If all three of the following apply, then assume that you do not need to repeat the analog output software test. However, by process of elimination, you failed the digital I/O software test the last time you tried. Go to step 5 and repeat the digital I/O software test.
      – Your board has analog outputs (for example, you have a KPCI-3108 board).
      – You have done the analog output software test at least once.
      – Your software passed the analog output software test the last time you tried.
    - If your board does not have analog outputs (for example, a KPCI-3107 board) then by process of elimination, you failed the digital I/O software test the last time you tried. Go to step 5 and repeat the digital I/O software test.
13. You arrived at this point from step 8, because presumably you have a commercial or otherwise unmodifiable applications program that is assumed to be proven. Contact the maker of your software to determine whether you have a version designed to work with the KPCI-3108 version of DriverLINX. For example, not all versions of TestPoint will work with KPCI-3108 DriverLINX. Also, check whether the program is installed correctly.
14. Select your next step in Scheme C based on the criteria given in the following alternatives:
    - If you are certain at this point that your application program is the correct version AND is properly installed, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem. Also, contact Keithley if you have been unable to find out elsewhere whether you have the correct version of software.
    - If you are uncertain at this point that your application program is properly installed, then reinstall it now. When you are satisfied that it is properly installed, go to step 11 and retry selected I/O software tests.

Problem isolation Scheme D: expansion slot connectors

In Scheme D, you further check and try to remedy apparent expansion slot malfunctions. Refer to Figure 6-13.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

Figure 6-13
Problem isolation Scheme D: expansion slot connectors

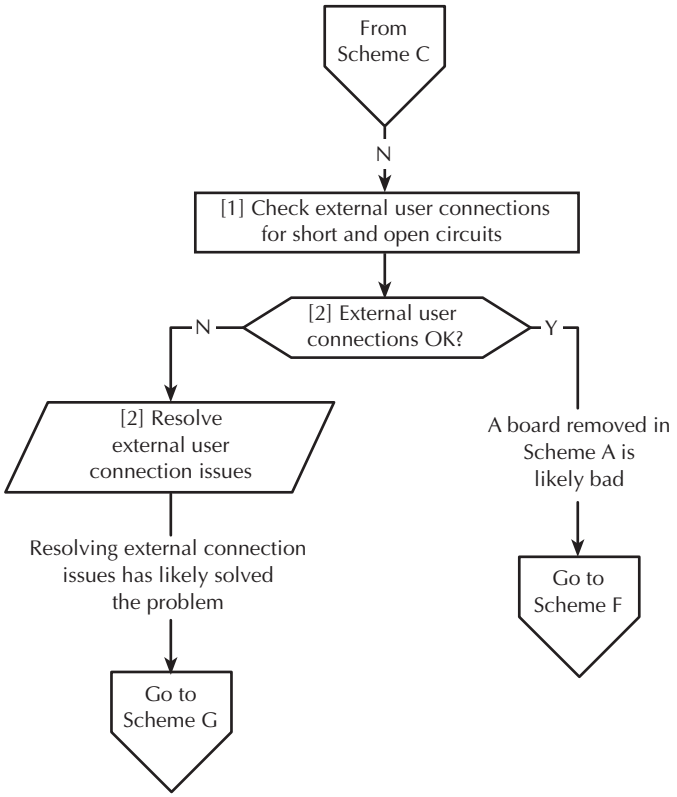

From Scheme A
Determine the PCI devices already found by the host computer (ref. Scheme A, Step 5)
In slot where board was not detected as a new PCI device in Scheme A (only one assumed), remove and securely reseat the OK board at least two times; leave it seated
Check for a new PCI device (ref. Scheme A, Step 7)
OK board now found as a new PCI device in the slot tested?
Y
Improper seating/wiping of PCI connection was likely the problem, which has apparently been fixed
Go to Scheme G
N
Is there a free PCI slot from which KPCI-3108 Series boards were not removed in Scheme A?
N
Service the malfunctioning PCI slot connector: clean contacts/repair bad solder joints/replace, as required
Y
Determine what PCI devices have already been found by computer (ref. Scheme A, Step 5)
Install OK board in a free PCI slot from which KPCI-3108 Series boards were not removed in Scheme A
OK board found as new PCI device (ref. Scheme A, Step 7)?
N
Get Keithley help
Y
Determine what PCI devices have already been found by computer (ref. Scheme A, Step 5)
Install OK board in serviced PCI slot connector
OK board found as new PCI device (ref. Scheme A, Step 7)?
Y
N
Get Keithley help
Replace OK board used for tests with the board removed in Scheme A
Malfunctioning PCI connector was likely the problem; board is apparently now installed in a good PCI connector
Go to Scheme G

Problem isolation Scheme E: user wiring

In Scheme E, after having eliminated other problem causes, you physically check your external connections to see if they are the problem cause. Refer to Figure 6-14.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

Figure 6-14
Problem isolation Scheme E: user wiring


From Scheme C
N
[1] Check external user connections for short and open circuits
[2] External user connections OK?
N
Y
[2] Resolve external user connection issues
Resolving external connection issues has likely solved the problem
Go to Scheme G
A board removed in Scheme A is likely bad
Go to Scheme F

Follow these amplified instructions as you perform Scheme E:

1. Check the I/O connections between each external signal source and the screw terminal accessory, one at a time, for short circuits and open circuits. If KPCI-3108 boards were installed in more than one PCI slot, check the I/O connections for all boards.

NOTE *Do not connect the screw terminal accessory to the board during this scheme.*

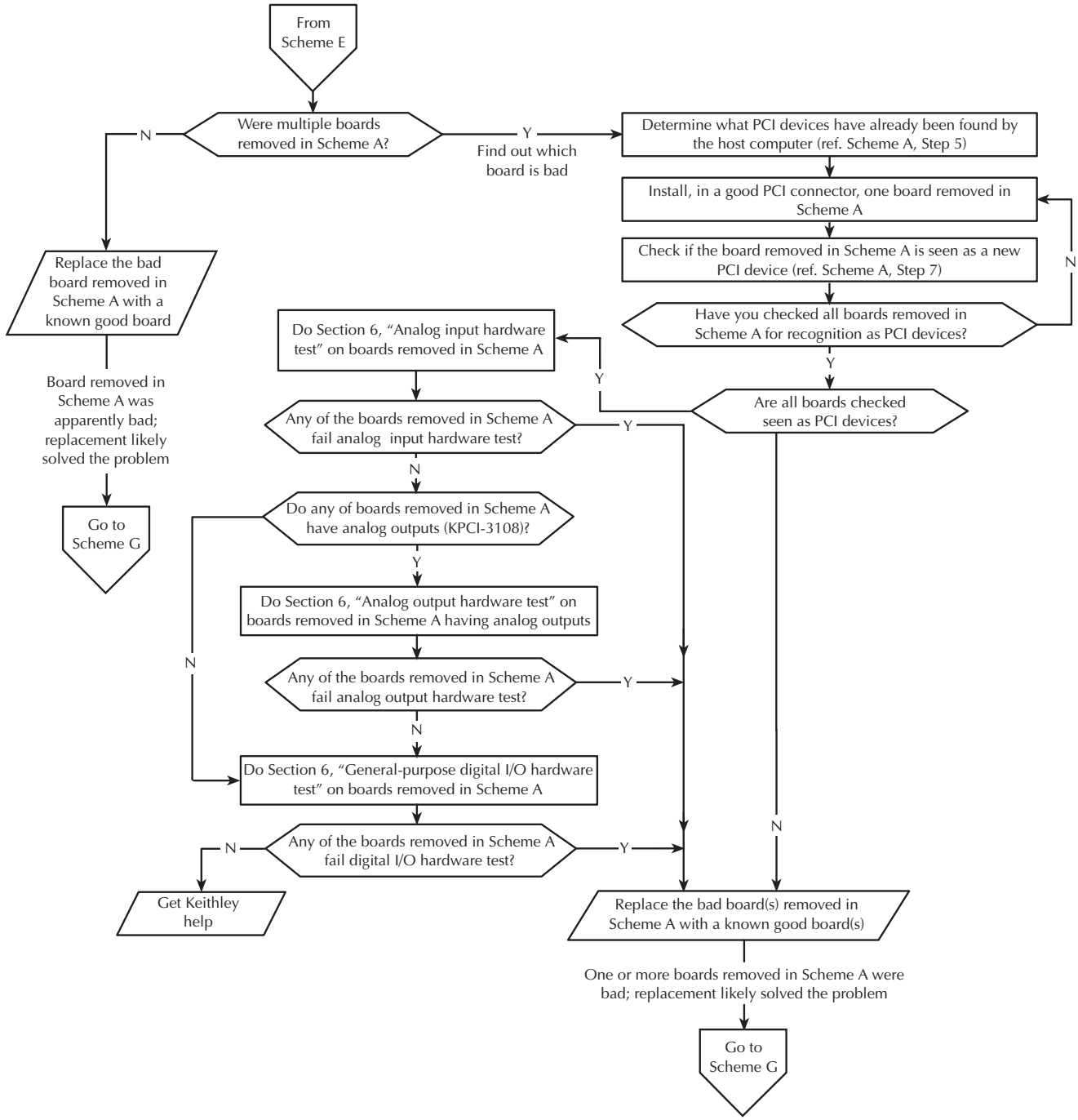
2. Based on the results of step 1, do the following:
   - If any external I/O connections are found to be faulty, assume that the problem was caused by the faulty connections, then proceed as follows:
     a. Correct the faulty external connections.
     b. Skip to "Problem isolation Scheme G: verification of problem solution."
   - If all external I/O connections are found to be normal, then, by process of elimination, the KPCI-3108 board(s) originally installed in the computer is likely the cause of the problem. Continue with "Problem isolation Scheme F: the board."

Problem isolation Scheme F: the board

In Scheme F, after having eliminated other problem causes, you assume that KPCI-3108 hardware malfunctions are at fault. If only one KPCI-3108 board was installed, you replace or repair it. If more than one KPCI-3108 board was installed, you use PCI connection tests, and if necessary I/O tests, to find which board is bad. Refer to Figure 6-15.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

Figure 6-15
Problem isolation Scheme F: the board

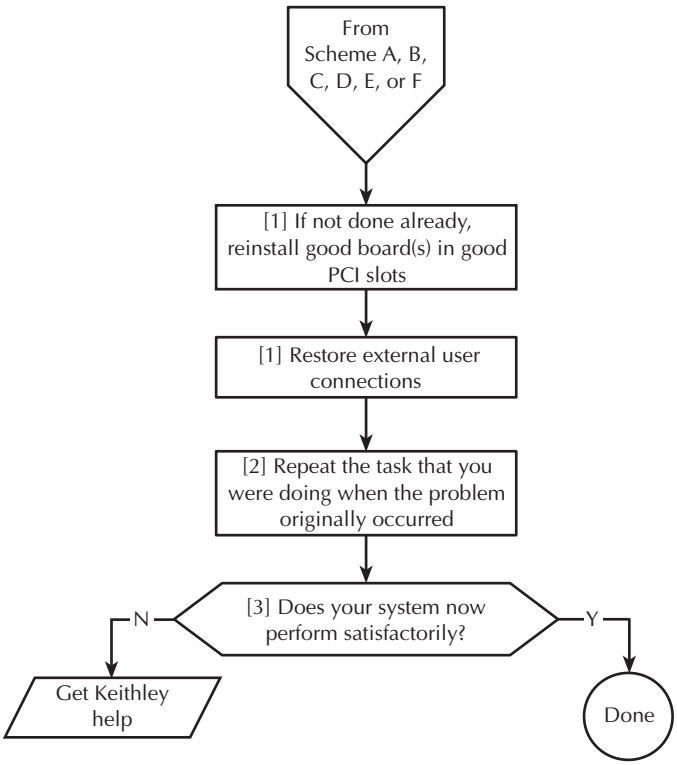

From Scheme E
Were multiple boards removed in Scheme A?
N
Y
Find out which board is bad
Determine what PCI devices have already been found by the host computer (ref. Scheme A, Step 5)
Install, in a good PCI connector, one board removed in Scheme A
Check if the board removed in Scheme A is seen as a new PCI device (ref. Scheme A, Step 7)
Have you checked all boards removed in Scheme A for recognition as PCI devices?
N
Y
Are all boards checked seen as PCI devices?
Y
N
Replace the bad board removed in Scheme A with a known good board
Board removed in Scheme A was apparently bad; replacement likely solved the problem
Go to Scheme G
Do Section 6, "Analog input hardware test" on boards removed in Scheme A
Any of the boards removed in Scheme A fail analog input hardware test?
Y
N
Do any of boards removed in Scheme A have analog outputs (KPCI-3108)?
Y
N
Do Section 6, "Analog output hardware test" on boards removed in Scheme A having analog outputs
Any of the boards removed in Scheme A fail analog output hardware test?
Y
N
Do Section 6, "General-purpose digital I/O hardware test" on boards removed in Scheme A
Any of the boards removed in Scheme A fail digital I/O hardware test?
N
Y
Get Keithley help
Replace the bad board(s) removed in Scheme A with a known good board(s)
One or more boards removed in Scheme A were bad; replacement likely solved the problem
Go to Scheme G

Problem isolation Scheme G: verification of problem solution

In Scheme G, you put your system back together and verify that it works, after apparently resolving the problem in prior schemes. Refer to Figure 6-16 and the written amplification following it.

NOTE *This is not a stand-alone procedure. Use it only when it is called for by another procedure.*

Figure 6-16
Problem isolation Scheme G: verification of problem solution


From Scheme A, B, C, D, E, or F
[1] If not done already, reinstall good board(s) in good PCI slots
[1] Restore external user connections
[2] Repeat the task that you were doing when the problem originally occurred
[3] Does your system now perform satisfactorily?
N
Y
Get Keithley help
Done

Follow these amplified instructions as you perform Scheme G:

1. Assuming that the problem has been resolved, do the following:
   a. Turn OFF the computer.
   b. Install good KPCI-3108 boards in good slots.
   c. Reconnect all external circuits. If you left external circuits connected to the screw terminal accessory, connect the accessory to your board. If you disconnected external circuits from the screw terminal accessory, reconnect them and the accessory as discussed in Section 3, "lnstallation."
   d. Turn ON the computer and start your data acquisition software.
2. Repeat the task that you were doing with your data acquisition system when the problem occurred, and observe the performance.

3. Based on the results of step 2, do one of the following:
   - If the system now performs satisfactorily, you have successfully isolated and corrected the problem.
   - If the system still does not perform satisfactorily, then the cause of your problem may be outside the scope of these diagnostics. Read the instructions in "Technical support," and then contact Keithley for help in isolating the cause of your problem.

Specified hardware I/O tests

The tests in this section check whether the analog and digital I/O of the board work properly. The I/O are tested using proven DriverLINX utilities, thereby bypassing any unresolved application software issues. These tests are intended to be used when specified in the preceding "Systematic problem isolation" procedure. However, they may also be used at any time for general functional checks of your KPCI-3108 board.

NOTE *During these tests, disconnect all user circuits from board, except for connections specified in individual test procedures.*

Analog input hardware test

The analog input test checks whether the analog inputs, particularly the instrumentation amplifier and A/D converter, are working correctly. In this test, a voltage applied to KPCI-3108 channel 01 is measured using the on-screen digital voltmeter utility that is supplied with DriverLINX. In the same way, channel 00 is grounded and checked for offset voltage. One voltage measurement and one grounded-input measurement are sufficient because of the following:

- All analog channels are connected to the same instrumentation amplifier and A/D converter, via the multiplexer.
- The multiplexer is unlikely to be a problem source.

Both the voltage and grounded-input measurements are made in the single-ended input mode.

NOTE *During this test, ensure that no user circuits are connected to the KPCI-3108 board, except for analog input connections specified for the test.*

The analog input test is a functional test, not a calibration check, although readings from a properly calibrated board should correspond to a known test voltage within the accuracy specifications of the board. If you wish to check and adjust the accuracy, refer to Section 5, "Calibration."

Equipment for the analog input hardware test

The following equipment is needed for the analog input test:

- A voltage source supplying a known voltage at <5V. Refer to Table 6-2 for more details.
- (Optional) A Digital Voltmeter (DVM) or a Digital Multimeter (DMM) to accurately determine the voltage of the voltage source.
- An STP-36 or STP-36/C screw terminal accessory wired as shown in Table 6-2. (These are the same connections as made for the analog input *software* test.)

  If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Table 6-2
Wiring for analog input hardware test

Connect this test voltage…	**…between this analog input terminal…**	**…and an analog ground terminal.**
0V, via a short between the analog input terminal and ground	33 (Channel 00 HI)	17 or 18
<+5V from one of the following: • A battery • An isolated power supply • A voltage divider — e.g. 10kΩ or 20kΩ— between the +5V board power output (terminal 25) and analog ground (terminal 17 or 18)*	32 (Channel 01 HI)	17 or 18

*For example, composed of two 5kΩ or 10kΩ resistors. Observe the ***CAUTION*** below.

CAUTION **If you use the +5V board power to energize a voltage divider, ensure that the +5V board power terminal cannot accidentally short to ground. A short to ground can damage one or more of the following: the screw terminal accessory, the board, the computer.**

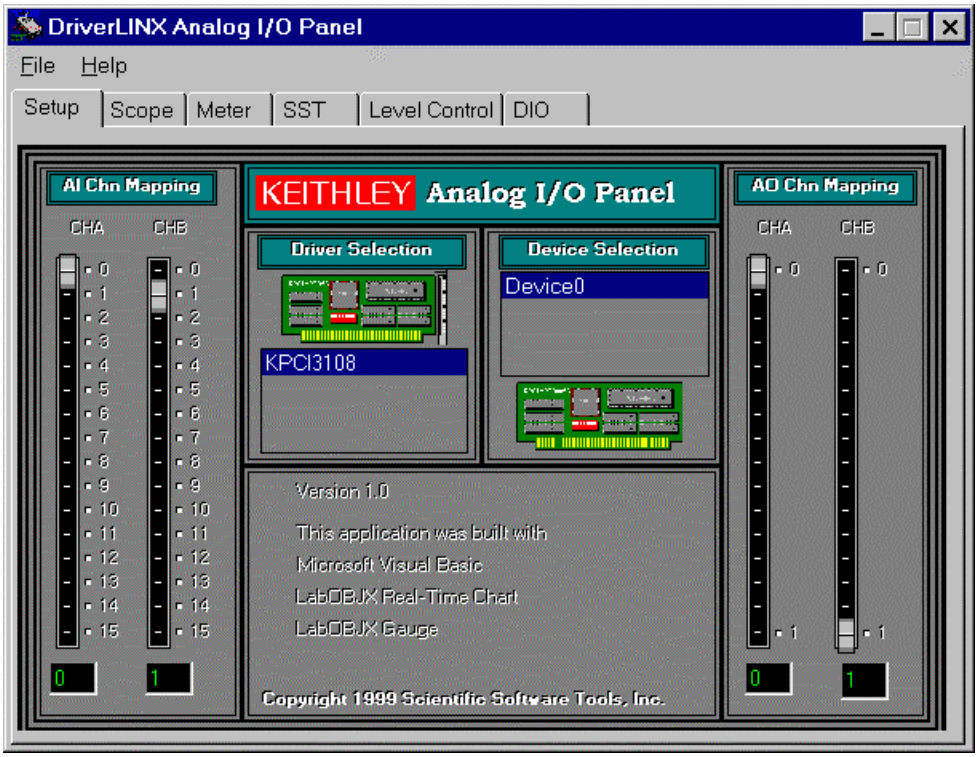
Procedure for the analog input hardware test

Perform the analog input test as follows:

1. Turn OFF the host computer.
2. Wire a screw terminal accessory as described under "Equipment for the analog input hardware test."
3. Connect the screw terminal accessory, as wired in step 2, to the KPCI-3108 upper "Analog" I/O connector.
4. Turn ON the host computer and boot Windows 95, 98, or NT.
5. In the **Start** menu, click **Programs.**
6. Find the **DriverLINX → Test Panels** folder, under which you should find the **AIO Panel** entry.

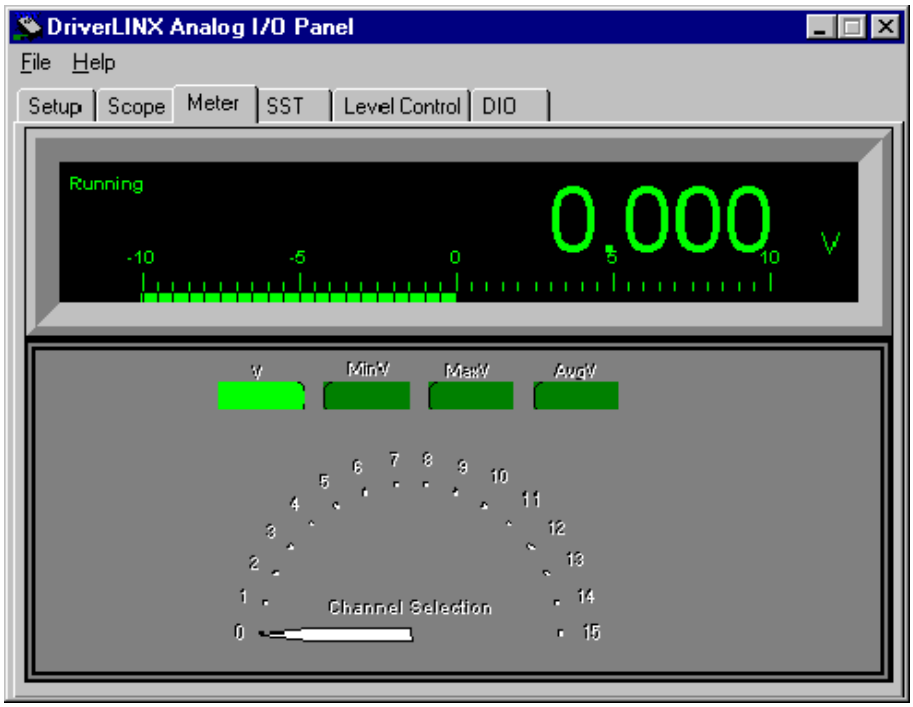
7. Click on the **AIO Panel** entry. The Analog I/O Panel setup screen appears.
   - If a KPCI-3108 board is the only computer board that is installed in your computer under DriverLINX, Figure 6-17 is similar to what you will see.
   - If more than one type of board is installed in your computer under DriverLINX, the Analog I/O Panel may appear similar to Figure 6-17, but with multiple drivers listed under **Driver Selection** and/or multiple devices listed under **Device Selection** (for example, **Device0, Device1**, etc.). Your board type and device number may not be displayed initially, and fewer tabs may be displayed at the top of the screen than in Figure 6-17. If so, click the scroll buttons next to the Driver Selection and Device Selection text boxes until your KPCI-3108 board type and device number are displayed. All six tabs will then be displayed.

Figure 6-17
Analog I/O Panel setup screen example



8. Click the **Meter** tab. An on-screen digital voltmeter appears, displaying the voltage connected to Channel 00. Because Channel 00 is grounded, the displayed voltage should be nominally zero, as illustrated in Figure 6-18.

Figure 6-18
On-screen digital voltmeter display example: channel 0 connected to ground

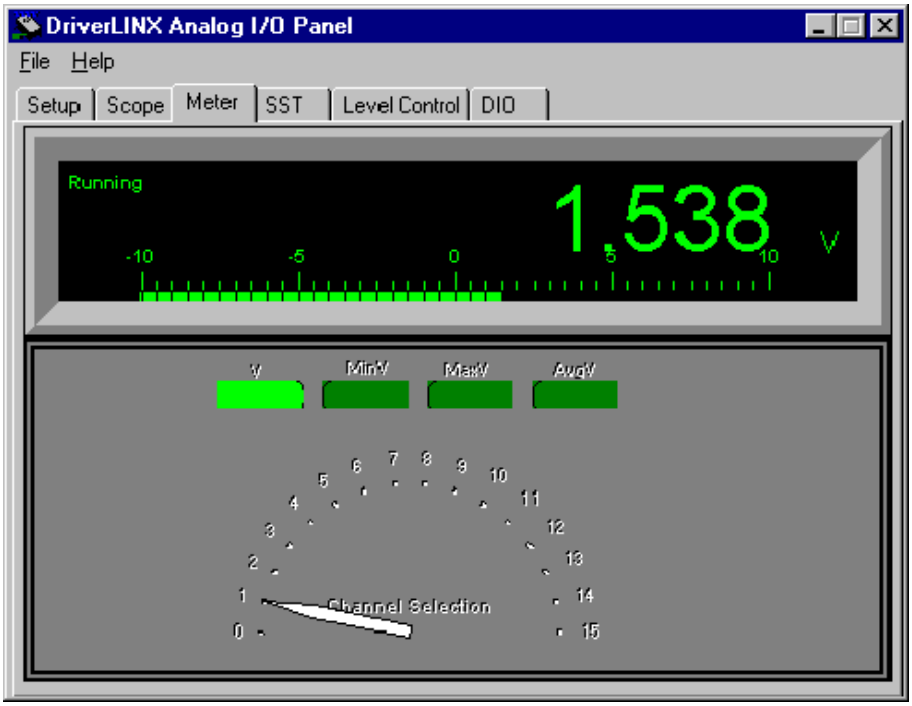


9. Using your mouse, move the **Channel Selection** pointer of the on-screen digital panel meter to 1.

NOTE *To move the **Channel Selection** pointer, you must contact the wide part of the pointer with the tip of the cursor.*

The on-screen digital voltmeter now displays the voltage connected to channel 01. Figure 6-19 shows the on-screen digital voltmeter and the voltage that was displayed when channel 01 was connected to a flashlight battery.

Figure 6-19
On-screen digital voltmeter display example: channel 1 connected to flashlight battery


DriverLINX Analog I/O Panel
File Help
Setup Scope Meter SST Level Control DIO
Running
1.538
V
-10 -5 0 5 10
V MinV MaxV AvgV
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
Channel Selection

10. Based on the displayed voltages in steps 8 and 9, act as follows:
    - If the channel 00 voltage displayed in step 8 is not 0V and/or if the channel 01 voltage displayed in step 9 does not nominally agree with the applied voltage, then your board apparently has analog input problems. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the Analog input hardware test.
    - If the channel 00 voltage displayed in step 8 is 0V and the channel 01 voltage displayed in step 9 nominally agrees with the applied voltage, then the analog inputs are apparently satisfactorily. Stop here, and the return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the Analog input hardware test.

NOTE *If the analog inputs appear to work satisfactorily but the displayed channel 00 and channel 01 voltages appear to be nominally outside specified limits, you may wish to calibrate your board after concluding the "Systematic problem isolation" procedure. For board specifications refer to Appendix A. For calibration procedures, refer to Section 5, "Calibration."*

Analog output hardware test

This test applies only to a board having analog outputs (the KPCI-3108).The analog output test checks whether the two digital-to-analog converters (DACs) of the board are working correctly. Zero voltages are set at the two analog outputs, using the on-screen level control utility that is supplied with DriverLINX. The two output voltages are then measured with a digital voltmeter to verify reasonable DAC offsets. Similarly, a mid-range voltage is set for each of the two analog outputs and the procedure is repeated to verify proper digital to analog conversion.

NOTE *During this test, ensure that no user circuits are connected to the KPCI-3108 board, via the required screw terminal accessory, except for analog output connections specified for the test.*

The analog output test is primarily a functional test, not a calibration check, although measured outputs from a properly calibrated board should correspond to DAC settings, within the accuracy specifications of the board. If you wish to check and adjust the accuracy, refer to Section 5, "Calibration."

Equipment for the analog output hardware test

The following equipment is required to perform the analog output test:

- A Digital Voltmeter (DVM) or a Digital Multimeter (DMM) set to the 10V range.
- An STP-36 or STP-36/C screw terminal accessory, to which you connect the DVM/DMM as indicated in Table 6-3.These are the same connections as made for the analog output *software* test.

  If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Table 6-3
Terminals on accessory for connection during analog output hardware test

To check this analog output…	…the DVM or DMM will be connected to these terminals	
	Analog output screw terminal	Analog-ground screw terminal
Analog output 0	36	17 or 18
Analog output 1	35	17 or 18

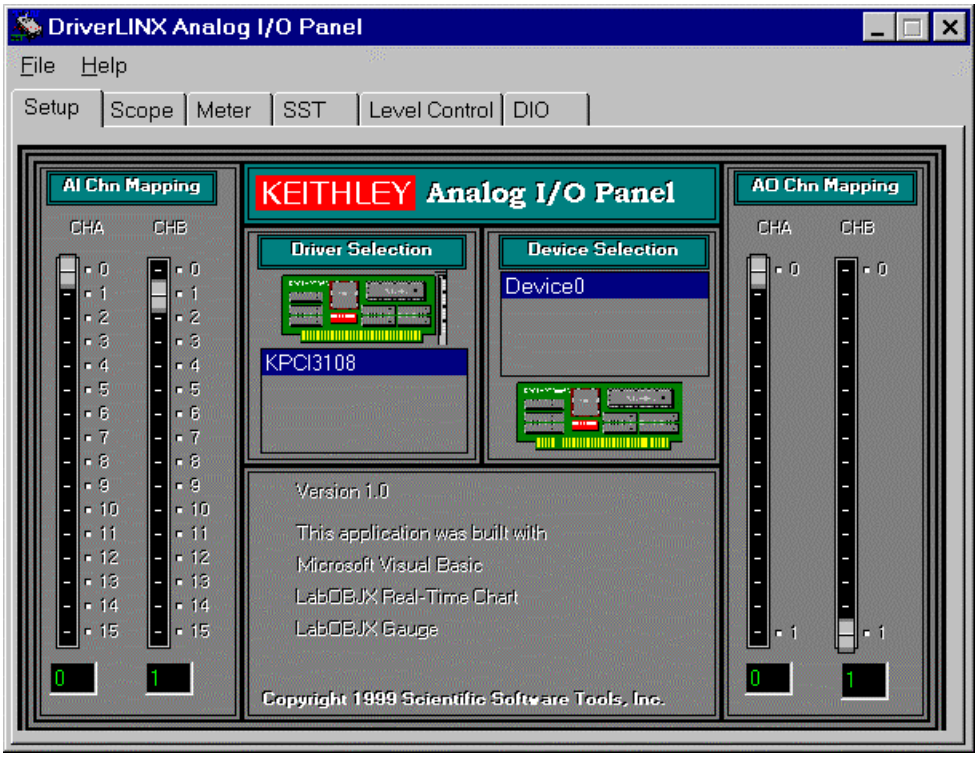
CAUTION **The following test procedure involves changing DVM/DMM connections while the computer and KPCI-3108 board are powered. Take care not to short analog outputs to the adjacent +10 V reference terminal or nearby ground terminal. Shorting the analog outputs can damage the digital-to-analog converters (DACs). As a precaution, do the following:**

- **Before powering the computer, connect the DVM/DMM negative lead to a ground screw terminal.**
- **After powering the computer, connect the DVM/DMM positive lead to each specified analog output screw terminal by touching the tip of the lead to the screw head of the screw terminal (for example, via a probe).**

Procedure for the analog output hardware test

1. Turn OFF the host computer.
2. Connect the negative lead of the DVM/DMM to a ground terminal of the screw terminal accessory, as indicated in Table 6-3.
3. Connect the STP-36 or STP-36/C screw terminal accessory to the KPCI-3108 upper "Analog" I/O connector.
4. Turn ON the host computer and boot Windows 95, 98, or NT.
5. In the **Start** menu, click **Programs.**
6. Find the **DriverLINX** → **Test Panels** folder, under which you should find the **AIO Panel** entry.
   - If a KPCI-3108 board is the only computer board that is installed under DriverLINX, Figure 6-20 shows a setup screen similar to what you will see.

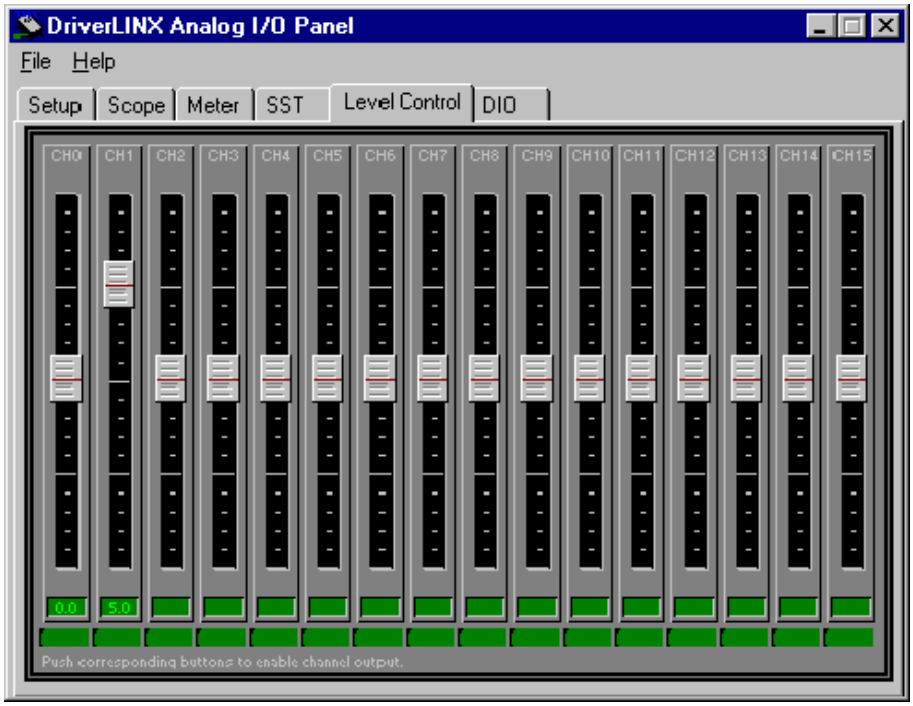
Figure 6-20
Analog I/O Panel setup screen example when only a KPCI-3108 board is installed under DriverLINX



- If more than one type of board is installed in your computer under DriverLINX, the Analog I/O Panel may appear similar to Figure 6-20, but with multiple drivers listed under **Driver Selection** and/or multiple devices listed under **Device Selection** (for example, **Device0, Device1**, etc.) Your board type and device number may not be displayed initially, and fewer tabs may be displayed at the top of the screen than in Figure 6-20. If so, click the scroll buttons next to the **Driver Selection** and **Device Selection** text boxes until your KPCI-3108 board type and device number are displayed. All six tabs will then be displayed.

7. Click the **Level Control** tab. The on-screen analog-output level control appears, similar to Figure 6-21.

Figure 6-21
On-screen analog-output level control


DriverLINX Analog I/O Panel
File Help
Setup Scope Meter SST Level Control DIO
CH0 CH1 CH2 CH3 CH4 CH5 CH6 CH7 CH8 CH9 CH10 CH11 CH12 CH13 CH14 CH15
0.0
5.0
Push corresponding buttons to enable channel output.

8. Using your mouse, slide the CH0 level control button until the tiny display at the bottom of the level control reads **0.0** (volts).
9. In the same way, set the CH1 level control so that its tiny display reads **0.0** (volts).
10. Measure and compare the analog output voltages as indicated in Table 6-4:
    a. Measure the voltages at analog outputs 0 and 1 with your DVM/DMM.
    b. Compare the voltages you measured in step 10a with the voltages you set via the analog-output level control.

Table 6-4
Test connections and readings for zero-voltage analog output connected to upper "Analog" I/O connector

	…connect the DVM or DMM to these terminals on an STP-36 or STP-36/C accessory:		If board works correctly, the following voltages should agree:	
To test this analog output…	**Analog output screw terminal**	**Analog-ground screw terminal**	**Level control setting**	**Voltage reading at DVM or DMM**
Analog output 0	36	17 or 18	0.0V	0.0V
Analog output 1	35		0.0V	0.0V

11. Using your mouse, slide the CH0 and CH1 level control buttons until the tiny displays at the bottoms of the level controls read 5.0.
12. Measure and compare the analog output voltages as indicated in Table 6-5:
    a. Measure the voltages at analog outputs 0 and 1 with your DVM/DMM.
    b. Compare the voltages you measured in step 12a with the voltages you set via the analog-output level control.

Table 6-5
Test connections and readings for mid-range analog output connected to upper "Analog" I/O connector

	…connect the DVM or DMM to these terminals on an STP-36 or STP-36/C accessory:		**If board works correctly, the following voltages should agree:**	
To test this analog output…	**Analog output screw terminal**	**Analog-ground screw terminal**	**Level control setting**	**Voltage reading at DVM or DMM**
Analog output 0	36	17 or 18	5.0V	5.0V
Analog output 1	35		5.0V	5.0V

13. Based on the measured voltages in steps 10 and 12, take action as follows:
    - If the voltages measured with the DVM/DMM do not agree with the level control settings, then there is an apparent problem with the analog output part of your board. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the Analog output hardware test.
    - If the voltages measured with the DVM/DMM agree with level control settings, then the analog outputs are working satisfactorily. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the Analog output hardware test.

NOTE *If the analog outputs appear to work satisfactorily, but some measured analog output voltages are outside the accuracy limits specified in Appendix A, consider calibrating your board after concluding the "Systematic problem isolation" procedure. For calibration procedures, refer to Section 5, "Calibration."*

General-purpose digital I/O hardware test

This test checks whether the general-purpose digital input and output circuits of the board are operating properly.

Test summary

The following summarizes the test procedure:

- Wire an STP-36 or STP-36/C screw terminal accessory in a loop-back configuration. Connect the channel 0 digital I/O terminals, bit-for-bit, to the channel 3 digital I/O terminals. Connect the channel 1 terminals, bit-for-bit, to the channel 2 terminals. See Figure 6-22 for the channel and bit number of each terminal on the screw terminal accessory. See Figure 6-23 for the loop-back wiring schematic. (These are the same connections as made for the general-purpose digital I/O *software* test.)

Figure 6-22
Channel and bit numbers for STP-36 and STP-36/C screw terminal accessories

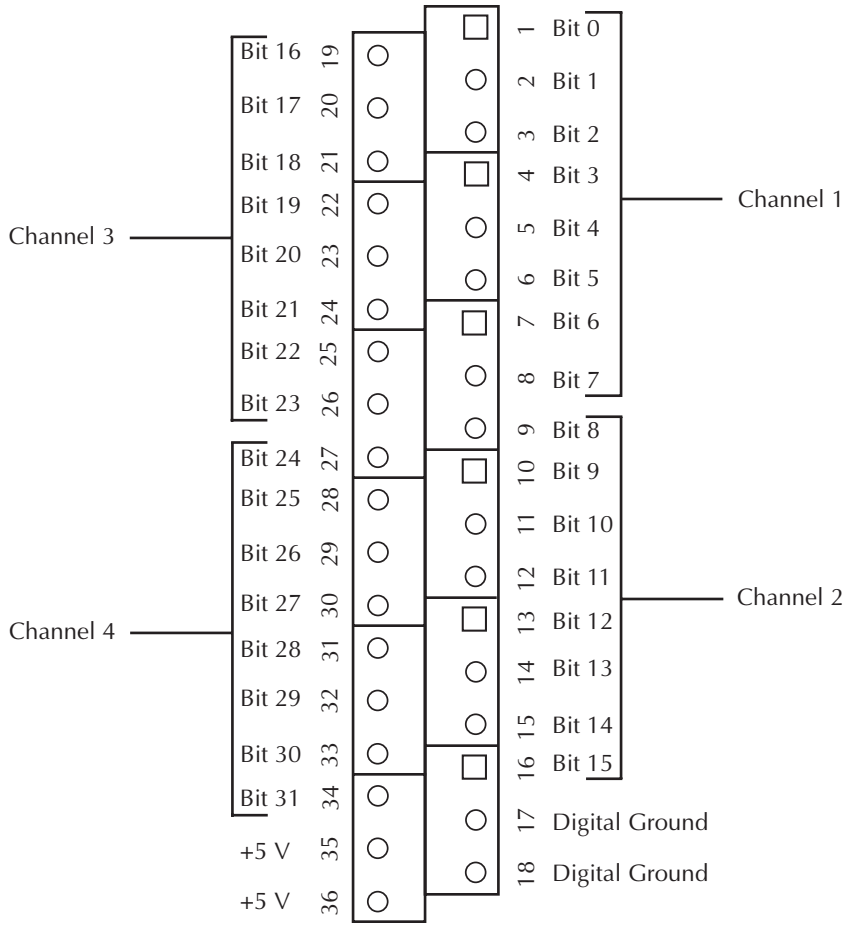
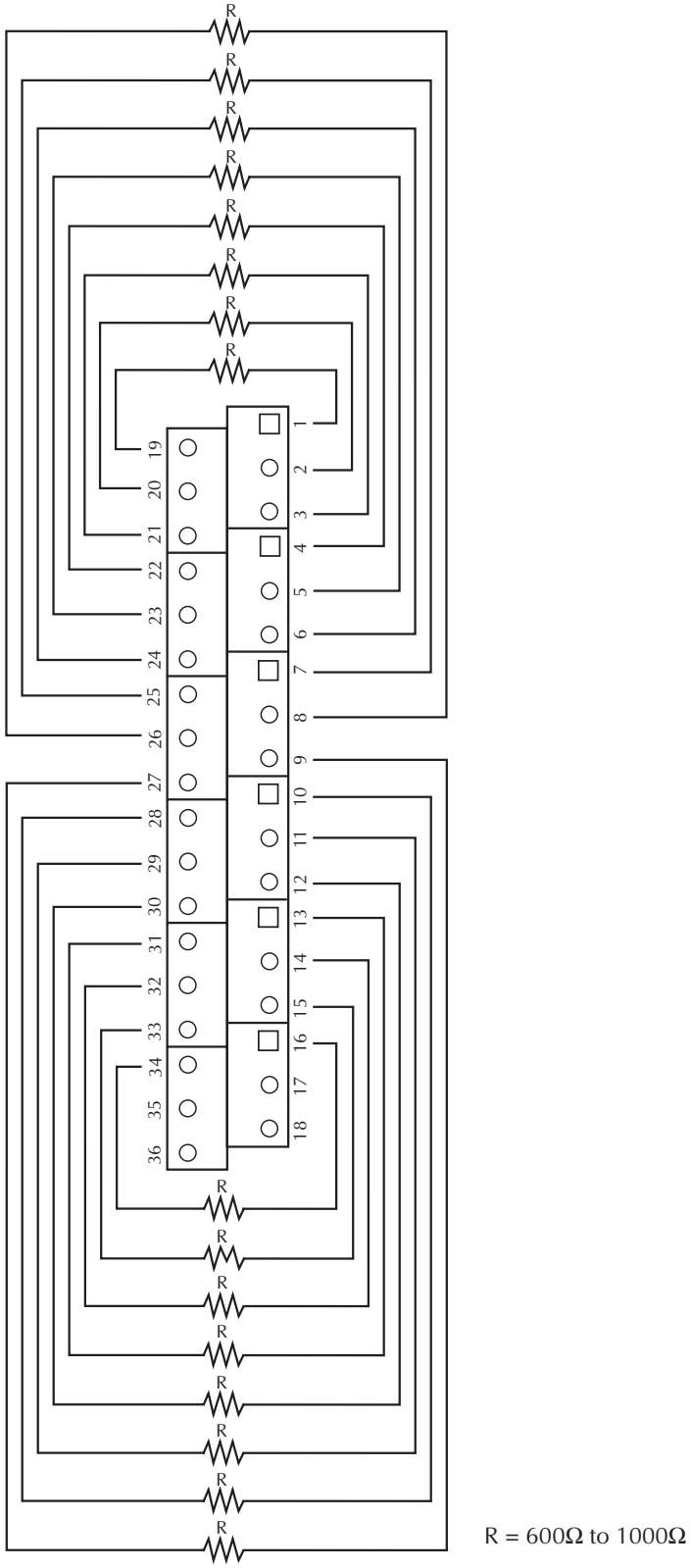


Figure 6-23
Loop-back wiring for general-purpose digital I/O hardware and software test



R = 600Ω to 1000Ω

- Using a DriverLINX graphical interface, configure the channel 0 and 1 bits as outputs and the channel 2 and 3 bits as inputs.
- Using the same DriverLINX graphical interface, set the channel 0 and 1 outputs in a particular bit pattern and check channels 2 and 3 inputs for the same bit pattern. Repeat, using a second bit pattern.

The digital I/O of the board is performing satisfactorily if all bits respond appropriately. The specified bit patterns check both for direct ON/OFF response and for shorts between bits.

Equipment for the general-purpose digital I/O hardware test

All I/O is set and read using the DriverLINX Digital Input/Output test panel, and no instruments are required. However, you must wire an STP-36 or STP-36/C screw terminal accessory in the loop-back configuration shown in Figure 6-23. If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Procedure for the general-purpose digital I/O hardware test

Perform the I/O hardware test as follows:

1. Turn OFF the host computer.
2. If a screw terminal accessory is attached to the upper "Analog" I/O connector of the KPCI-3108 I/O board, remove it. No circuits should be connected to the "Analog" I/O connector during these tests.
3. Wire an STP-36 or STP-36/C screw terminal accessory as described in Figure 6-23.
4. Attach the wired screw terminal accessory to the lower "Digital" I/O connector of the KPCI-3108 board. Refer to "Connecting interface accessories to a KPCI-3108 board" in Section 3 of this manual.
5. Turn ON the host computer and boot Windows 95, 98, or NT.
6. In the **Start** menu, click **Programs.**
7. Find the **DriverLINX → Test Panels** folder, under which you should find the **AIO Panel** entry.
8. Click on the **AIO Panel** entry. The Analog I/O Panel setup screen appears.
   - If a KPCI-3108 board is the only computer board that is installed in your computer under DriverLINX, Figure 6-24 is similar to what you will see.
   - If more than one type of board is installed in your computer under DriverLINX, the Analog I/O Panel may appear similar to Figure 6-24, but with multiple drivers listed under **Driver Selection** and/or multiple devices listed under **Device Selection** (for example, **Device0, Device1**, etc.) Your board type and device number may not be displayed initially, and fewer tabs may be displayed at the top of the screen than in Figure 6-24. If so, click the scroll buttons next to the Driver Selection and Device Selection text boxes until your KPCI-3108 board type and device number are displayed. All six tabs will then be displayed.
9. Click the **DIO** tab. An on-screen digital I/O controller appears, similar to Figure 6-25.

Figure 6-24
Analog I/O Panel setup screen when only a KPCI-3108 board is installed under DriverLINX

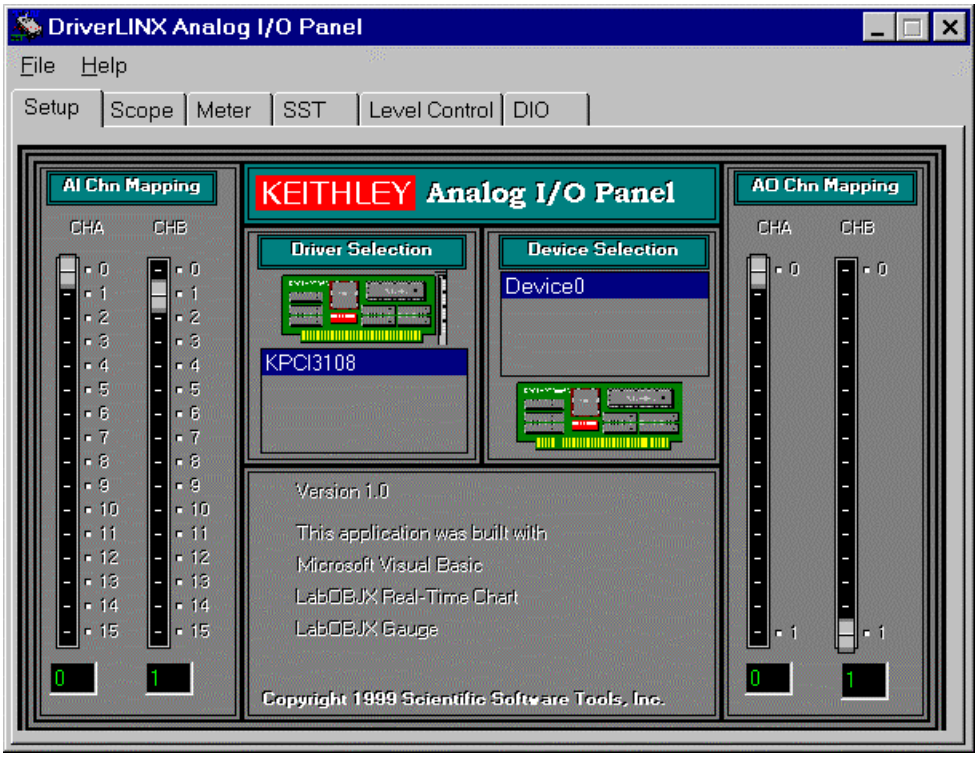
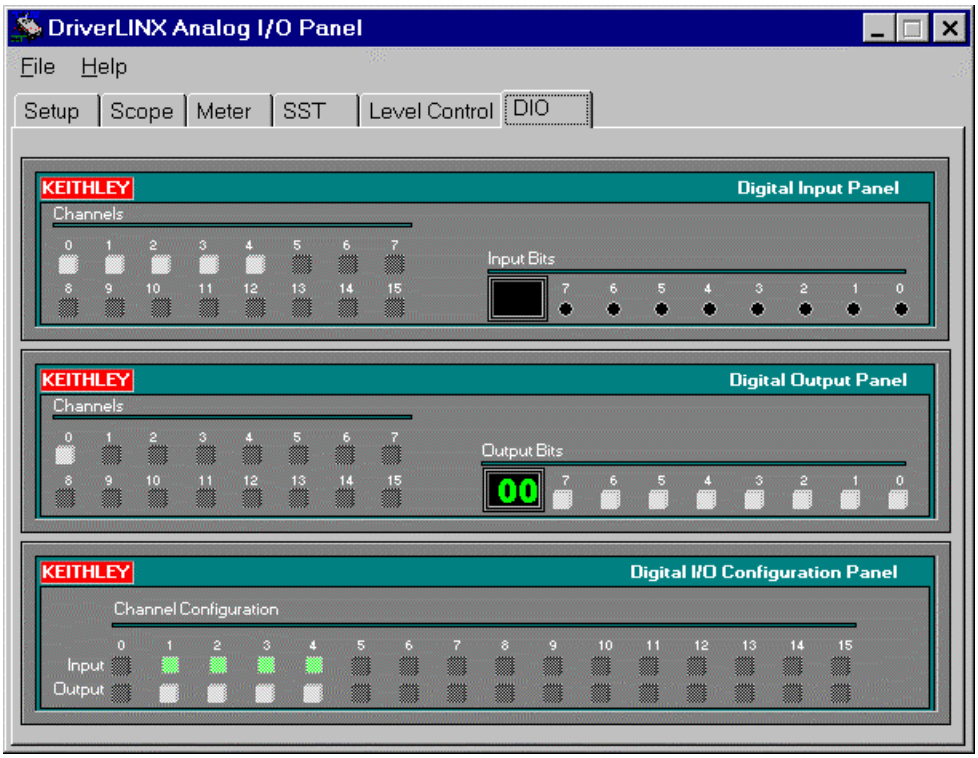


Figure 6-25
The on-screen digital I/O controller



NOTE *The on-screen digital I/O controller works as follows:*

- *Channel 0 refers to the twelve multi-function digital I/O bits. These bits may be manipulated with the digital I/O controller only when the multi-function bits are configured as general-purpose bits.*
- *Channels 1 to 4 refer to the four 8-bit general-purpose registers in the KPCI-3108. Bits displayed on the* **Digital Input Panel** *and the* **Digital Output Panel** *are numbered 0-7 for every channel—instead of 0-7 for channel 0, 8-15 for channel 1, 16-23 for channel 2, and 24-31 for channel 3 as for the KPCI-3108 "Digital" I/O connector. Refer to Table 6-6.*

Table 6-6
Bit numbering on Digital I/O Panel vs. "Digital" I/O connector

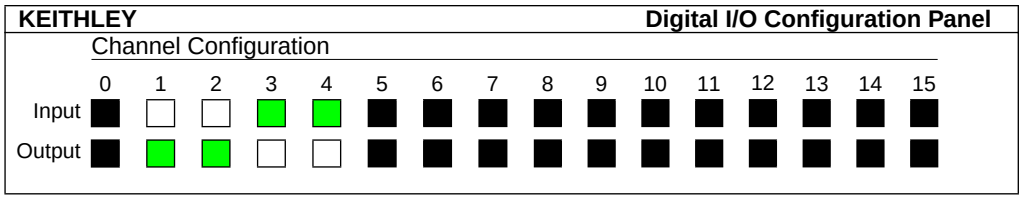
Channel 1 bit numbers		Channel 2 bit numbers		Channel 3 bit numbers		Channel 4 bit numbers	
On I/O panels	**At "Digital" connector**	**On I/O panels**	**At "Digital" connector**	**On I/O panels**	**At "Digital" connector**	**On I/O panels**	**At "Digital" connector**
0	0	0	8	0	16	0	24
1	1	1	9	1	17	1	25
2	2	2	10	2	18	2	26
3	3	3	11	3	19	3	27
4	4	4	12	4	20	4	28
5	5	5	13	5	21	5	29
6	6	6	14	6	22	6	30
7	7	7	15	7	23	7	31

- *Invalid channels and settings appear as dark gray squares. For example:*
  - *Non-existent channels always appear as dark gray squares.*
  - *In the Digital I/O Configuration Panel, Channel 0, corresponding to the twelve multi-function digital I/O bits, appears as dark gray squares. The configuration of the twelve bits is fixed; six are always inputs and six are always outputs.*
- *Valid channels and settings appear as white squares when OFF and green squares when ON (When the manual is printed in black and white, valid channels and settings appear as white squares when OFF and as light gray squares when ON).*
- *The two-digit numeric displays under* **Input Bits** *and* **Output Bits** *show the hexadecimal values of the adjacent bit patterns.*
- *To configure a valid channel either for input or output, use the* **Digital Channel Configuration Panel.** *Click on either the* **Input** *or* **Output** *square below the channel number.*
- *To turn ON output-channel bits, use the* **Digital Output Panel.** *First select the channel number of the bits to be turned on by clicking on the appropriate square under* **Channels***. Then, turn ON a bit by clicking the appropriate square under* **Output Bits***. Turn OFF a bit in the same way.*

- *To read an input-channel bit, use the* **Digital Input Panel**. *First select the channel number to be checked by clicking the appropriate square under* **Channels**. *Then, read the numbered bit under* **Input Bits**. *OFF input bits appear as black dots and ON input bits appear as green dots. (When the manual is printed in black and white, OFF input bits appear as black dots and ON input bits appear as light gray dots.)*

10. Under **Digital I/O Configuration Panel,** configure channels 1 to 4 as shown in Figure 6-26.

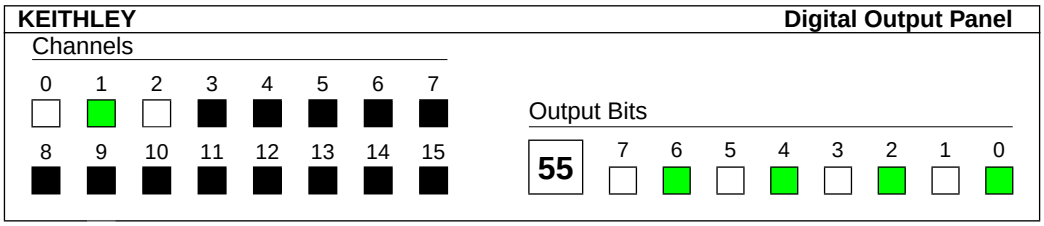
Figure 6-26
Configuring the digital I/O channels as inputs and outputs



NOTE *In Figure 6-26 and subsequent drawings of digital I/O controller panels, the squares below invalid channels are colored black instead of dark gray—for clarity when the manual is printed in black and white.*

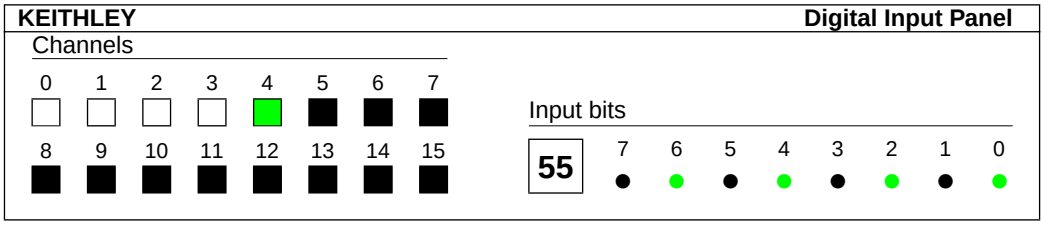
11. In the **Digital Output Panel** under **Channels,** click on channel **1** as shown in Figure 6-27.

Figure 6-27
Configuring channel 1 for output bit pattern A



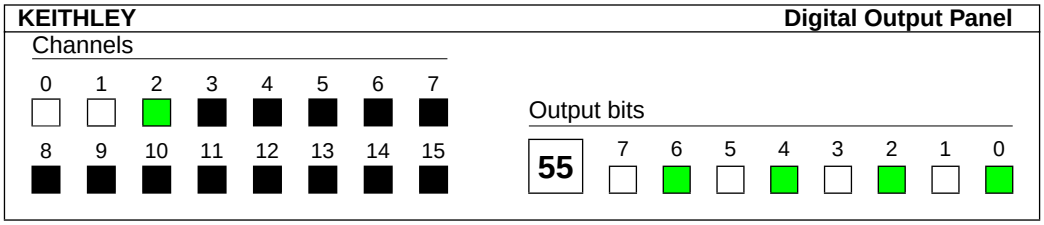
12. In the **Digital Output Panel** under **Output Bits,** set the bits of channel **1** for bit pattern A as shown in Figure 6-27.
13. In the **Digital Input Panel** under **Channels**, click on channel **4** as shown in Figure 6-28.

Figure 6-28
Proper response of channel 4 input bits when channel 1 output bits are set to bit pattern A



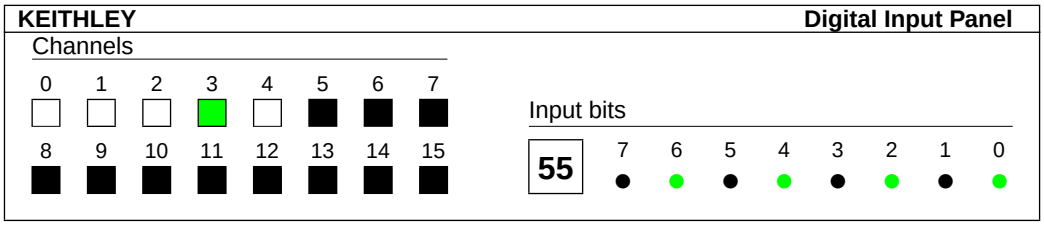
14. In the **Digital Input Panel** under **Input bits** observe the bit pattern. Figure 6-28 shows the proper response.
    - If the observed input bit patterns are not the same as shown in Figure 6-28, the digital I/O is not functioning properly. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the General-purpose digital I/O hardware test.
    - If the input bit patterns are the same as shown in Figure 6-28, continue with step 15.
15. In the **Digital Output Panel** under **Channels,** click on channel **2** as shown as shown in Figure 6-29.

Figure 6-29
Configuring channel 2 for output bit pattern A



16. In the **Digital Output Panel** under **Output Bits**, configure channel **2** for bit pattern A as shown in Figure 6-29.
17. In the **Digital Input Panel** under **Channels**, click on channel **3** as shown in Figure 6-30.

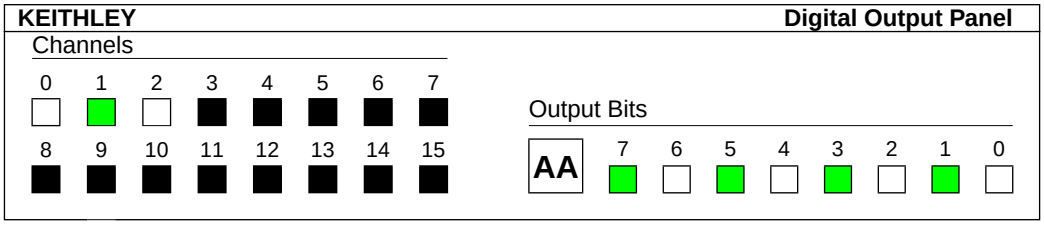
Figure 6-30
Proper response of channel 3 input bits when channel 2 output bits are set to bit pattern A



18. In the **Digital Input Panel** under **Input bits** observe the bit pattern. Figure 6-30 shows the proper response.
    - If the observed input bit patterns are not the same as shown in Figure 6-30, the digital I/O is not functioning properly. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the General-purpose digital I/O hardware test.
    - If the input bit patterns are the same as shown in Figure 6-30, continue with step 19.

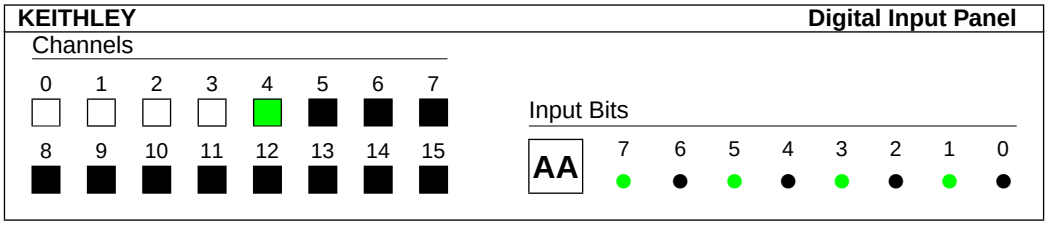
19. In the **Digital Output Panel** under **Channels,** click on channel **1** as shown as shown in Figure 6-31.

Figure 6-31
Configuring channel 1 for output bit pattern B



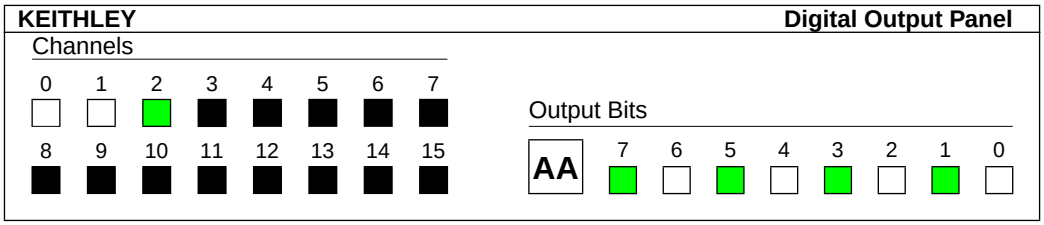
20. In the **Digital Output Panel** under **Output Bits,** set the bits of channel **1** for bit pattern B as shown in Figure 6-31.
21. In the **Digital Input Panel** under **Channels**, click on channel **4** as shown in Figure 6-32.

Figure 6-32
Proper response of channel 4 bits when channel 1 output bits are set to bit pattern B



22. In the **Digital Input Panel** under **Input bits** observe the bit pattern. Figure 6-32 shows the proper response.
    - If the observed input bit patterns are not the same as shown in Figure 6-32, the digital I/O is not functioning properly. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the General-purpose digital I/O hardware test.
    - If the input bit patterns are the same as shown in Figure 6-32, continue with step 23.
23. In the **Digital Output Panel** under **Channels,** click on channel **2** as shown in Figure 6-33.

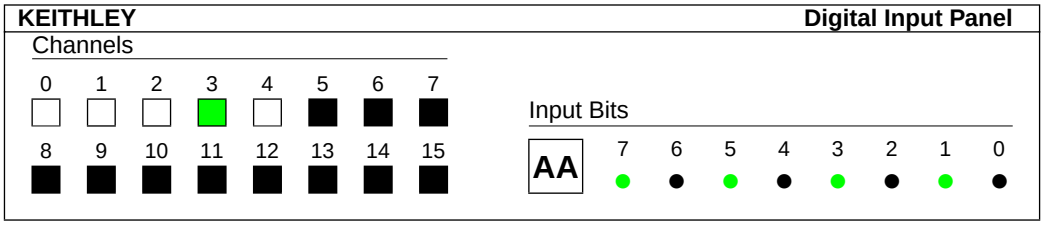
Figure 6-33
Configuring channel 2 for output bit pattern B



24. In the **Digital Output Panel** under **Output Bits,** set the bits of channel **2** for bit pattern B as shown in Figure 6-33.

25. In the **Digital Input Panel** under **Channels**, click on channel **3** as shown in Figure 6-34.

Figure 6-34
Proper response of channel 3 bits when channel 2 output bits are set to bit pattern B



26. In the **Digital Input Panel** under **Input bits** observe the bit pattern. Figure 6-34 shows the proper response.
    - If the observed input bit patterns are not the same as shown in Figure 6-34, the digital I/O is not functioning properly.
    - If the input bit patterns are the same as shown in Figure 6-34, the digital I/O is functioning properly.
27. Stop here, and return to the problem isolation step in "Problem isolation Scheme F: the board" that asked you to perform the General-purpose digital I/O hardware test.

NOTE *When the multi-function bits are configured as general-purpose bits, a similar test of the twelve multi-function digital I/O bits can be performed with the on-screen digital I/O controller. Wire loop-back connections at an STP-36 accessory between same-numbered input and output bits. (If you **ensure** that outputs are always wired only to inputs, no protective series resistors are required. If two output bits are wired together and both are turned ON without adequate current limiting, damage will result.) Turn input bits 0, 2, and 4 ON and look for an identical output bit pattern. Repeat, turning input bits 1, 3, and 5 ON.*

Specified software I/O tests

The tests in this section check whether your application software correctly performs analog and digital I/O tasks. The I/O are tested using a KPCI-3108 board known to work properly, thereby bypassing potential board problems. These tests are intended to be used when specified in the preceding "Systematic problem isolation" procedure.

NOTE *During these tests, disconnect all user circuits from the board, except for connections specified in individual test procedures.*

Analog input software test

This basic analog input test checks whether your application software correctly monitors DC analog inputs. You ground analog channel 0, apply a DC voltage to channel 1, and measure the results.

NOTE *During this test, ensure that no user circuits are connected to the KPCI-3108 board, via the required screw terminal accessory, except for analog input connections specified for the test.*

NOTE *The analog input test is a software function test, not a calibration check, although readings from a properly calibrated board should correspond to a known test voltage within the accuracy specifications of the board. If you wish to check and adjust the accuracy, refer to Section 5, "Calibration."*

NOTE *The analog input software test is only a basic check of your application software. You are encouraged to perform additional tests that exercise your software more thoroughly.*

Equipment for the analog input software test

The following equipment is needed for the analog input test:

- A voltage source supplying a known voltage at <5V. Refer to Table 6-7 for more details.
- (Optional) A Digital Voltmeter (DVM) or a Digital Multimeter (DMM) to accurately determine the voltage of the voltage source.
- An STP-36 or STP-36/C screw terminal accessory wired as shown in Table 6-7. This is the same wiring scheme as used in the analog input *hardware* tests.

  If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Table 6-7
Wiring for analog input software test

Connect this test voltage…	**…between this analog input terminal…**	**…and an analog ground terminal.**
0V, via a short between the analog input terminal and ground	33 (Channel 00 HI)	17 or 18
<+5V from one of the following: • A battery • An isolated power supply • A voltage divider — e.g. 10kΩ or 20kΩ— between the +5V board power output (terminal 25) and analog ground (terminal 17 or 18)*	32 (Channel 01 HI)	17 or 18

*For example, composed of two 5kΩ or 10kΩ resistors. Observe the ***CAUTION*** below.

CAUTION **If you use the +5V board power to energize a voltage divider, ensure that the +5V board power terminal cannot accidentally short to ground. A short to ground can damage one or more of the following: the screw terminal accessory, the board, the computer.**

Procedure for the analog input software test

Perform the analog input test as follows:

1. Turn OFF the host computer.
2. Wire a screw terminal accessory as described under "Equipment for the analog input software test."
3. Connect the screw terminal accessory, as wired in step 2, to the KPCI-3108 board upper "Analog" I/O connector.
4. Turn ON the host computer and boot Windows 95, 98, or NT.
5. Start DriverLINX and your application software.
6. Set your application software to measure and display/report voltages from analog input channels 00 and 01 at a rate suitable for monitoring DC signals. Configure your system as follows:
   - The ±5V input range
   - Single ended input
7. Based on the displayed/reported voltages in step 6, act as follows:
   - If the measured channel 00 voltage is not 0V and/or if the measured channel 01 voltage does not agree with the applied voltage, then there could be a problem with the way your application software program interfaces with DriverLINX or the way it deals with analog input data from the board. Stop here, and return to the systematic problem isolation Scheme C, step 1, where you were directed to do analog input software tests.
   - If the measured channel 00 voltage is 0V and the measured channel 01 voltage agrees with the applied voltage, then your software is treating DC analog input data correctly. Stop here, and return to the systematic problem isolation Scheme C, step 1, where you were directed to do analog input software tests.

Analog output software test

This test applies only to a board having analog outputs (the KPCI-3108).This basic analog input test checks whether your application software correctly sets direct current (DC) analog output voltages. You set zero volts at the two analog outputs, using your application software. The two output voltages are then measured with a digital voltmeter to verify reasonable DAC offsets. Similarly, a mid-range voltage is set for each of the two analog outputs and the procedure is repeated.

NOTE *During this test, ensure that no user circuits are connected to the KPCI-3108 board, via the required screw terminal accessory, except for analog input connections specified for the test.*

The analog output software test is a software function test, not a calibration check. If you wish to check and adjust the accuracy, refer to Section 5, "Calibration."

The analog output software test is only a basic check of your application software. You are encouraged to perform additional tests that exercise your software more thoroughly.

Equipment for the analog output software test

The following equipment is required to perform the analog output test:

- A Digital Voltmeter (DVM) or a Digital Multimeter (DMM) set to the 10V range.
- An STP-36 or STP-36/C screw terminal accessory, to which you connect the DVM/DMM as indicated in Table 6-8.These are the same connections as made for the analog output *hardware* test.

  If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Table 6-8
Connection terminals for analog output software test

To check this analog output…	…the DVM or DMM will be connected to these terminals	
	Analog output screw terminal	Analog-ground screw terminal
Analog output 0	36	17 or 18
Analog output 1	35	17 or 18

CAUTION **The following test procedure involves changing DVM/DMM connections while the computer and KPCI-3108 board are powered. Be careful not to short analog outputs to the adjacent +10V reference terminal or nearby ground terminals. Shorting the analog outputs can damage the Digital-to-Analog Converters (DACs). As a precaution, do the following:**

- **Before powering the computer, connect the DVM/DMM negative lead to a ground screw terminal.**
- **After powering the computer, connect the DVM/DMM positive lead to each specified analog output screw terminal by touching the tip of the lead to the screw head of the screw terminal (for example, via a probe).**

Procedure for the analog output software test

1. Turn OFF the host computer.
2. Connect the negative lead of the DVM/DMM to a ground terminal of the screw terminal accessory, as indicated in Table 6-8.
3. Connect the STP-36 or STP-36/C screw terminal accessory to the KPCI-3108 I/O connector.
4. Turn ON the host computer and boot Windows 95, 98, or NT.
5. Start DriverLINX and your application software.
6. Set your application software to output 0V at analog outputs 0 and 1.

7. Measure and compare the analog output voltages as indicated in Table 6-9:
   a. Measure the voltages at analog outputs 0 and 1 with your DVM/DMM.
   b. Compare the voltages you measured in step 7a with the voltages you set via the analog-output level control.

Table 6-9
Test connections and readings for zero-voltage analog output

	…connect the DVM or DMM to these terminals on an STP-36 or STP-36/C accessory:		If board works correctly, the following voltages should agree:	
To test this analog output…	**Analog output screw terminal**	**Analog-ground screw terminal**	**Level control setting**	**Voltage reading at DVM or DMM**
Analog output 0	36	17 or 18	0.0V	0.0V
Analog output 1	35		0.0V	0.0V

8. Set your application software to output +5V at analog outputs 0 and 1.
9. Measure and compare the analog output voltages as indicated in Table 6-10:
   a. Measure the voltages at analog outputs 0 and 1 with your DVM/DMM.
   b. Compare the voltages you measured in step 9a with the voltages you set via the analog-output level control.

Table 6-10
Test connections and readings for mid-range analog output

	…connect the DVM or DMM to these terminals on an STP-36 or STP-36/C accessory:		If board works correctly, the following voltages should agree:	
To test this analog output…	**Analog output screw terminal**	**Analog-ground screw terminal**	**Output voltage setting**	**Voltage reading at DVM or DMM**
Analog output 0	36	17 or 18	+5V	+5V
Analog output 1	35		+5V	+5V

10. Based on the measured voltages in steps 7 and 9, take action as follows:
    - If the voltages measured with the DVM/DMM do not agree with the application software settings, then there could be a problem with the way your application software program interfaces with DriverLINX or the way it prepares the analog data being sent to the board. Stop here, and return to step 3 of "Problem isolation Scheme C: application software," where you were directed to do analog output software tests.
    - If the voltages measured with the DVM/DMM agree with your application software settings, then your software is probably working correctly with the analog outputs. Stop here, and return to step 3 of "Problem isolation Scheme C: application software," where you were directed to do analog output software tests.

General-purpose digital I/O software test

This test checks whether your application software is performing general-purpose digital I/O functions properly.

Test summary

The following summarizes the test procedure:

- Wire an STP-36 or STP-36/C screw terminal accessory in a loop-back configuration. Connect the channel 0 general-purpose digital I/O terminals, bit-for-bit, to the channel 3 general-purpose digital I/O terminals. Connect the channel 1 terminals, bit-for-bit, to the channel 2 terminals. See Figure 6-35 for the channel and bit number of each terminal on the screw terminal accessory. See Figure 6-36 for the loop-back wiring schematic. (These are the same loop-back connections as made for the general-purpose digital I/O *hardware* test.)

Figure 6-35
Channel and bit numbers for STP-36 and STP-36/C screw terminal accessories

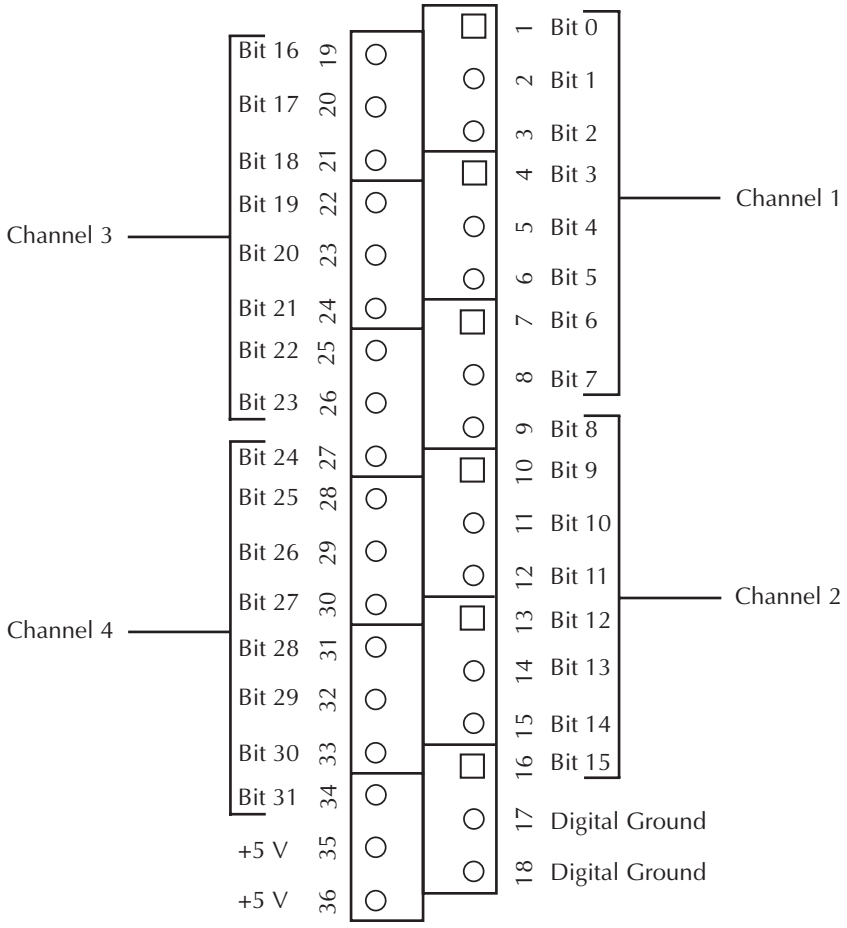
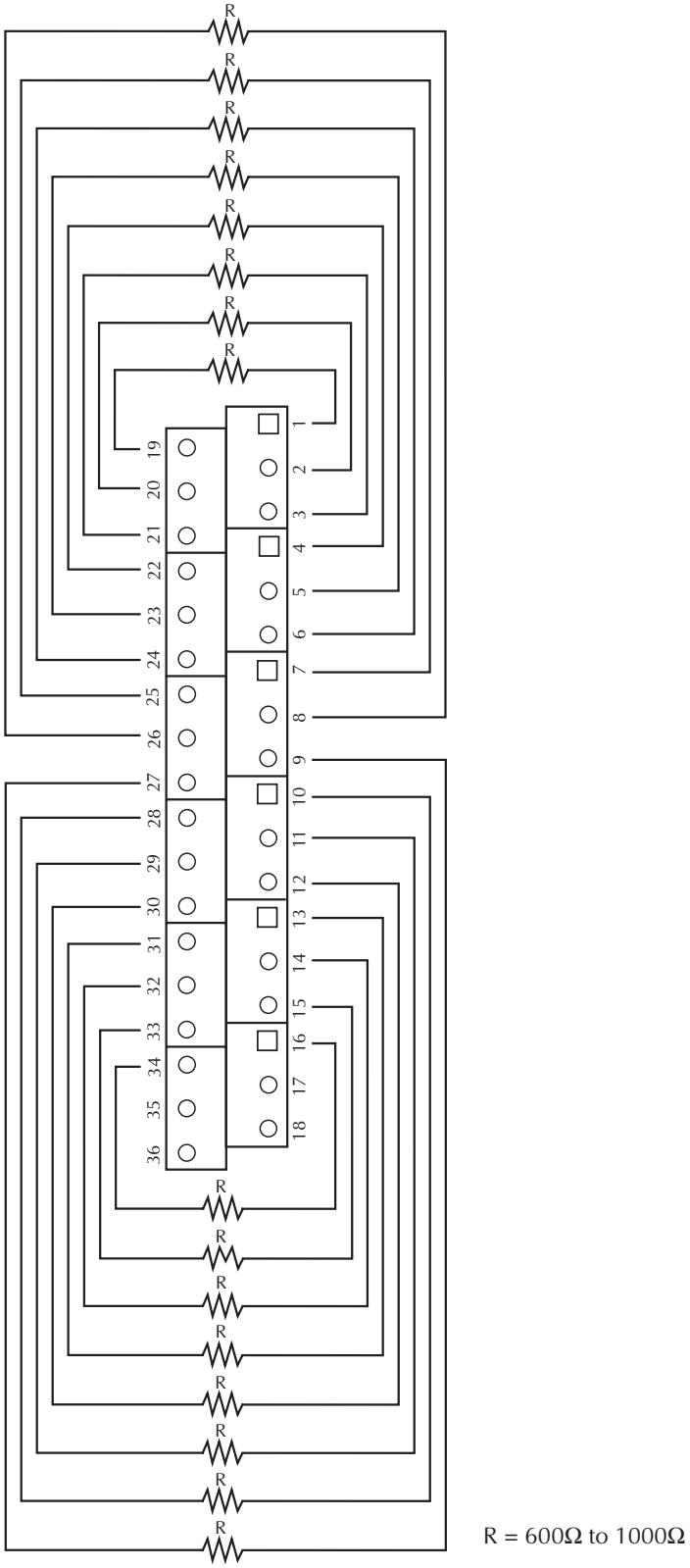


Figure 6-36
Loop-back wiring for general-purpose digital I/O hardware and software test



- Using your application software, configure the channel 0 and 1 bits as outputs and the channel 2 and 3 bits as inputs.
- Using your application software, set the channel 0 and 1 outputs in a particular bit pattern and check channels 2 and 3 inputs for the same bit pattern. Repeat, using a second bit pattern.

Your application software is performing general-purpose digital I/O satisfactorily if all bits respond appropriately.

Equipment for general-purpose digital I/O software test

All I/O is set and read using your application software; no instruments are required. However, you must wire an STP-36 or STP-36/C screw terminal accessory in the loop-back configuration shown in Figure 6-36. If possible, use a screw terminal accessory that is reserved for I/O tests. Avoid using a screw terminal accessory that is normally connected to your external circuits. You thereby avoid the extra labor and potential wiring errors involved in disconnecting and later reconnecting your external circuits.

Procedure for general-purpose digital I/O software test

NOTE *The bit patterns prescribed in this procedure are shown graphically as follows:*

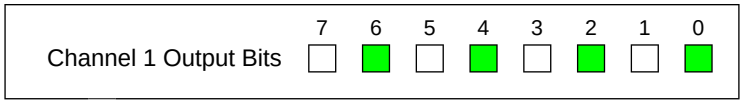
- *OFF bits appear as white squares*
- *ON bits appear as green squares when the manual is viewed in color or as light gray squares when the manual is viewed in black and white.*

Perform the I/O hardware test as follows:

1. Turn OFF the host computer
2. If a screw terminal accessory is attached to the upper "Analog" I/O connector of the KPCI-3108 I/O board, remove it. No circuits should be connected to the "Analog" I/O connector during these tests.
3. Wire an STP-36 or STP-36/C screw terminal accessory as described in Figure 6-36.
4. Attach the wired screw terminal accessory to the lower "Digital" I/O connector of the KPCI-3108 board. Refer to "Connecting interface accessories to a KPCI-3108 board" in Section 3 of this manual.
5. Turn ON the host computer and boot Windows 95, 98, or NT.
6. Start DriverLINX and your application software.
7. Set up your application software to configure and monitor general-purpose digital I/O bits.
8. Using your application software, do the following:
   a. Configure general-purpose bits 0 to 7 (channel 1) as outputs.
   b. Configure general-purpose bits 8 to 15 (channel 2) as outputs.
   c. Configure general-purpose bits 16 to 23 (channel 3) as inputs.
   d. Configure general-purpose bits 24 to 31 (channel 4) as inputs.

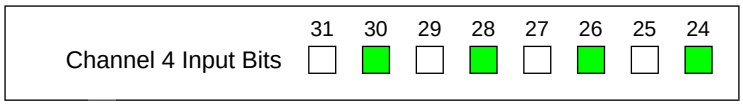
9. Using your application software, configure bits 0 to 7 (channel 1) for bit pattern A, as shown in Figure 6-37.

Figure 6-37
Configuring channel 1 for output bit pattern A



10. Using your application software, observe the channel 4 input bits. Figure 6-38 shows the proper response.

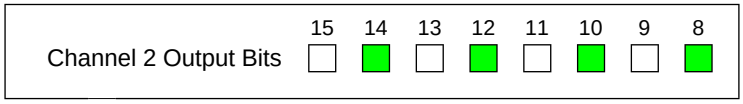
Figure 6-38
Proper response of channel 4 bits when channel 1 output bits are set to bit pattern A



- If the observed channel 4 input bit pattern is not the same as shown in Figure 6-38, your application software is not performing general-purpose digital I/O functions properly. Stop here, and return to step 5 of Scheme C in the "Systematic problem isolation" procedure.
- If the observed channel 4 input bit pattern is the same as shown in Figure 6-38, continue with step 11.

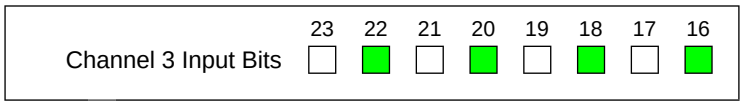
11. Using your application software, configure channel 2 for bit pattern A, as shown in Figure 6-39.

Figure 6-39
Configuring channel 2 for output bit pattern A



12. Using your application software, observe the channel 3 input bits. Figure 6-40 shows the proper response.

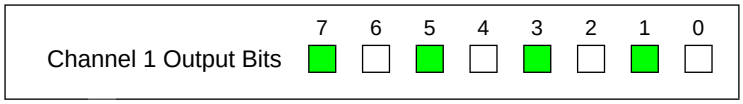
Figure 6-40
Proper response of channel 3 bits when channel 2 output bits are set to bit pattern A



- If the observed channel 3 input bit pattern is not the same as shown in Figure 6-40, your application software is not performing general-purpose digital I/O functions properly. Stop here, and return to step 5 of Scheme C in the "Systematic problem isolation" procedure.
- If the observed channel 3 input bit pattern is the same as shown in Figure 6-40, continue with step 13.

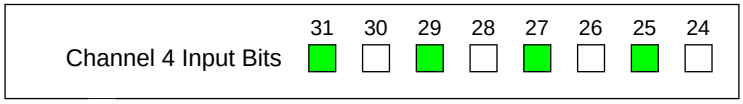
13. Using your application software, configure bits 0 to 7 (channel 1) for bit pattern B, as shown in Figure 6-41.

Figure 6-41
Configuring channel 1 for output bit pattern B



14. Using your application software, observe the channel 4 input bits. Figure 6-42 shows the proper response.

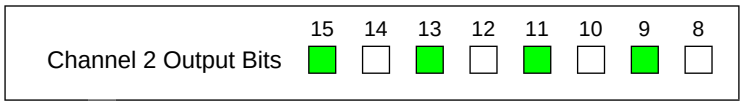
Figure 6-42
Proper response of channel 4 bits when channel 1 output bits are set to bit pattern B



- If the observed channel 4 input bit pattern is not the same as shown in Figure 6-42, your application software is not performing general-purpose digital I/O functions properly. Stop here, and return to step 5 of Scheme C in the "Systematic problem isolation" procedure.
- If the observed channel 4 input bit pattern is the same as shown in Figure 6-42, continue with step 15.

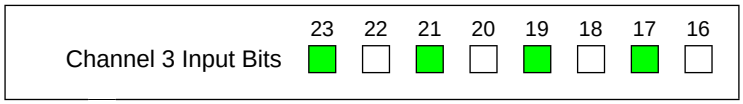
15. Using your application software, configure channel 2 for bit pattern B, as shown in Figure 6-43.

Figure 6-43
Configuring channel 2 for output bit pattern B



16. Using your application software, observe the channel 3 input bits. Figure 6-44 shows the proper response.

Figure 6-44
Proper response of channel 3 bits when channel 2 output bits are set to bit pattern B



- If the observed channel 3 input bit pattern is not the same as shown in Figure 6-44, your application software is not performing general-purpose digital I/O functions properly. Stop here, and return to step 5 of Scheme C in the "Systematic problem isolation" procedure.
- If the observed channel 3 input bit pattern is the same as shown in Figure 6-44, your application software is performing general-purpose digital I/O functions properly. Stop here, and return to step 5 of Scheme C in the "Systematic problem isolation" procedure.

Technical support

Before returning any equipment for repair, call Keithley for technical support at:

1-888-KEITHLEY
Monday - Friday, 8:00 a.m. - 5:00 p.m., Eastern Time

An applications engineer will help you diagnose and resolve your problem over the telephone. Please make sure that you have a record of any diagnostic tests that you have performed and the following information available before you call:

KPCI-3108 Series board configuration	Model	_____
	Serial #	_____
	Revision code	_____
	Number of channels	_____
	Input (S.E. or Diff.)	_____
	Mode (unipolar. or bipolar.)	_____
Computer	Manufacturer	_____
	CPU type	_____
	Clock speed (MHz)	_____
	MB of RAM	_____
	Video system	_____
	BIOS type	_____
Operating system	DOS version	_____
	Windows version	_____
		_____
Software package	Name	_____
	Serial #	_____
	Version	_____
	Invoice/Order #	_____
Compiler	Language	_____
(if applicable)	Manufacturer	_____
	Version	_____
Accessories	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____
	Type	_____

If a telephone resolution is not possible, the applications engineer will issue you a Return Material Authorization (RMA) number and ask you to return the equipment. Include the RMA number with any documentation regarding the equipment.

When returning equipment for repair, include the following information:

- Your name, address, and telephone number.
- The invoice or order number and date of equipment purchase.
- A description of the problem or its symptoms.
- The RMA number on the **outside** of the package.

Repackage the equipment, using the original anti-static wrapping, if possible, and handle it with ground protection. Ship the equipment to:

ATTN: RMA #_____
Repair Department
Keithley Instruments, Inc.
28775 Aurora Road
Cleveland, Ohio 44139

Telephone 1-888-KEITHLEY
FAX (440) 248-6168

NOTE *If you are submitting your equipment for repair under warranty, you must include the invoice number and date of purchase.*

To enable Keithley to respond as quickly as possible, you must include the RMA number on the outside of the package.

A
Specifications

Analog inputs

Number of Channels: 8 Differential or 16 Single Ended; Software Configurable in gain queue. Differential and Single-ended readings may be mixed.

A/D FIFO Buffer Size: 2048 Samples

Channel Gain Queue Length: 256 Entries

A/D Resolution: 16 Bits

Input Gain and Range:

Gain	Range Bipolar (V)	Range Unipolar (V)
1	±10	0 to 10
2	±5	0 to 5
4	±2.5	0 to 2.5
8	±1.25	0 to 1.25
10	±1	0 to 1
20	±0.5	0 to 0.5
40	±0.25	0 to 0.25
80	±0.125	0 to 0.125
100	±0.1	0 to 0.100
200	±0.05	0 to 0.050
400	±0.025	0 to 0.025
800	±0.0125	0 to 0.0125

Input Range Selection: Software selectable via channel gain queue entry. Unipolar and Bi-Polar readings may be mixed.

Input Overvoltage: Voltage between Input terminal and ground: ±35V continuous, powered; ±15V continuous, unpowered. Note: Input ground, chassis ground and earth ground are internally connected together.

Input Bias Current: ±1 nA typical per channel @ 25°C

Input Impedance: 1GΩ or greater in parallel with 200pF or less, all gains.

Single Channel Throughput: 100kS/s.

Scanning Throughput: Typical scanning rate at which switching introduces less than 0.015% of difference between adjacent readings, and typical % of difference between channels added at full speed.

Gain	Throughput	Error at full speed
1	100kS/s	0.01% @ 100kHz
2	100kS/s	0.01% @ 100kHz
4	100kS/s	0.01% @ 100kHz
8	100kS/s	0.01% @ 100kHz
10	100kS/s	0.01% @ 100kHz
20	80kS/s	0.02% @ 100kHz
40	50kS/s	0.03% @ 100kHz
80	35kS/s	0.04% @ 100kHz
100	35kS/s	0.02% @ 50kHz
200	20kS/s	0.1% @ 50kHz
400	20kS/s	0.1% @ 50kHz
800	20kS/s	0.12% @ 50kHz

Linearity:

Integral: ±1.5 LSB Max.
Differential: ±1 LSB Max.

Accuracy Bipolar:

Range	Resolution (µV)	25˚C ± 1˚C AZ on, 1Yr	Noise + Quantization (µV)		25˚C ± 25˚C AZ on, 1Yr
		%Reading + Offset	Single Point (typ.)	RMS	%Reading + Offset
±10V	305.17	0.0125% ±500µV	1500	350	0.0375% ±500µV
±5V	152.58	0.0125% ±250µV	750	175	0.0375% ±250µV
±2.5V	76.29	0.0125% ±120µV	375	90	0.0375% ±120µV
±1.25V	38.15	0.0125% ±75µV	200	50	0.0375% ±75µV
±1.0V	30.52	0.015% ±50µV	160	40	0.055% ±50µV
±0.5V	15.26	0.015% ±30µV	100	25	0.055% ±30µV
±0.25V	7.629	0.015% ±15µV	75	15	0.055% ±20µV
±0.125V	3.815	0.015% ±14µV	50	12	0.055% ±20µV
±0.100V	3.052	0.020% ±13µV	80	25	0.125% ±20µV
±0.050V	1.526	0.020% ±10µV	48	20	0.125% ±15µV
±0.025V	0.763	0.020% ±10µV	45	12	0.125% ±15µV
±0.0125V	0.382	0.020% ±10µV	40	10	0.125% ±15µV

Accuracy Unipolar:

Range	Resolution (µV)	25˚C ±1˚C AZ on, 1Yr	Noise + Quantization (µV)		25˚C ±25˚C AZ on, 1Yr
		%Reading + Offset	Single Point (typ.)	RMS	%Reading + Offset
0 to +10V	152.58	0.0125% ±350µV	750	125	0.0375% ±350µV
0 to +5V	76.29	0.0125% ±175µV	375	80	0.0375% ±175µV
0 to +2.5V	38.15	0.0125% ±75µV	190	50	0.0375% ±75µV
0 to +1.25V	19.07	0.0125% ±50µV	100	30	0.0375% ±50µV
0 to +1.0V	15.26	0.015% ±40µV	100	28	0.055% ±40µV
0 to +0.5V	7.629	0.015% ±25µV	75	25	0.055% ±25µV
0 to +0.25V	3.815	0.015% ±15µV	50	15	0.055% ±20µV
0 to +0.125V	1.907	0.015% ±13µV	50	12	0.055% ±20µV
0 to +0.100V	1.526	0.028% ±13µV	65	20	0.14% ±20µV
0 to +0.050V	0.763	0.028% ±10µV	50	15	0.14% ±15µV
0 to +0.025V	0.382	0.028% ±10µV	40	12	0.14% ±15µV
0 to +0.0125V	0.191	0.028% ±10µV	35	10	0.14% ±15µV

NOTE *Accuracies are based on an average of 10000 samples. Add noise to get maximum uncertainty of a single sample.*

Common Mode Rejection: Typical analog circuit rejection ratio with 10 V p-p sine wave excitation at 60 Hz.

Gain	CMRR (dB)
1	82.0
2	88.5
4	95.5
8	103.3
10	83.8
20	91.0
40	100.0
80	105.2
100	83.8
200	91.0
400	100.3
800	110.5

Data Transfer Modes: DMA (PCI Bus Master), Interrupt (Target-mode transfer), Polled (Target-mode transfer)

Analog outputs

Number of Channels:	Two
Resolution:	16 Bits
Maximum Update Rate:	500kS/s
Monotonicity:	16 Bits (DAC part specification — do not audit)
Range:	±10V, ±5V, 0-10V, 0-5V
Accuracy:	0.003% ±610µV, max. @ 25˚C
Temperature Coefficients:	
Offset:	310 µV / ˚C (typical)
Gain:	60 ppm / ˚C (typical)
Slew Rate:	5V/µs
Output Current:	±5 mA max
Protection:	Short-Circuit to ground
Maximum Capacitive Load:	100pF for 100kHz operation, typically, depending on ESR
Power Up:	0V (±75mV)
Data Transfer Modes:	DMA (PCI Bus Master), Interrupt (Target-mode transfer), Polled (Target-mode transfer)
D/A FIFO Buffer Size:	2048 Samples
D/A Control Modes:	
Target Mode:	Update either D/A
Paced Mode:	Update D/A converters in sequence
Burst Mode:	Update converters in sequence timed by burst counter
Worst Case Inter-Burst Skew:	2µsec, typical

Clock/Timer

Counter/Timers:

82C54:	Three 16-bit counters, each user configurable and user accessible.
Gain Queue:	Terminal counter in FPGA for each (A/D, D/A) queue
Burst Counter:	Separate counters for A/D and D/A burst rate
Time Divider:	Divides internal clock into 5MHz and 1MHz timebases

Timebases: Internal: 10 MHz

Internal Pacer Clock Rate: 100 kHz, max.
0.0012 Hz, min.

External Pacer Clock Rate: 100kHz, max.

External Pacer Clock Pulse Width: 10 ns, min.

Burst Clock Rate:

A/D:	100 kHz, max.
D/A:	500 kHz, max.

Trigger:

External Digital:	pre, post, about modes
Internal Software:	start, stop, pre, post, about modes
Internal Analog:	pre, post, about in DMA mode

External Trigger Pulse Width: 10ns, min.

Digital I/O

Input Bits: Six (6); User configurable as input timebase or gate for each of three 82C54 channels, external pacer for A/D or D/A, or External Digital Trigger. Can also be read by software in Target Mode

Input Low: V_{IL} = 0.8 V max.; I_{IL} = -0.2mA max.

Input High: V_{IH} = 2.0 V min.; I_{IH} = 20µA max.

Output Bits: Six (6); User configurable as Target mode outputs, 82C54 counter out bits, or trigger out. Four bits are used as EXP address bits when driving EXP-1600.

Output Low: V_{OL} = 0.5 V max.; I_{OL} = 8 mA max.

Output High: V_{OH} = 2.7 V min.; I_{OH} = -400µA max.

Data Transfer Mode: Target mode

Power on State: Input (High-Z)

Auxiliary High-Current Digital I/O

Number of Bits: 32 bits; four 74FCT652 bi-directional 8-bit registers. Each byte register is separately configurable as input or output.

Data Transfer Mode: Target mode

Input Low: V_{IL} = 0.8 V max.; I_{IL} = -0.2mA max.

Input High: V_{IH} = 2.0 V min.; I_{IH} = 20µA max.

Output Low: V_{OL} = 0.55 V max.; I_{OL} = 64mA max.

Output High: V_{OH} = 2.4 V min.; I_{OH} = -8mA max.
V_{OH} = 2.0 V min.; I_{OH} = -15mA max.

Power on State: Input (High-Z)

Power

Power Input:

+5 V: 430mA typ., 1.8A max., including user draw of 1A
+12 V: 400mA typ., 500mA max.

Power Output:

5 V: 3e1.0A max. (May also be limited by computer or bus capability)

Environment

Temperature, Operating: 0˚C to 50˚C

Temperature, Nonoperating: -20˚C to 70˚C

Humidity: 0 to 90% Relative (non-condensing), operating or nonoperating.

Dimensions: 8 in. (230mm) L x 4.25 in. (108mm) H x 0.75 in. (20mm) D Standard-Size PCI Short Card

Accessories

Termination:	STP-36 (Terminates CAB-1284 into 36 Screw Terminals) STA-3108-A1 (Provides 50-pin header for interfacing with EXP-1800) STA-3108-A2 (Provides 37-pin analog output connector compatible with DAS-16 pinout) STA-3108-A3 (Provides four connector for interfacing with MB-02) CONN-3108-D1 (Provides 50-pin digital connector compatible with KPCI-PIO-96 pinout
Signal Conditioning/ Expansion:	EXP-1800 (Through STA-3108 A1) MB-Series (Through CONN-3108-A2 and STA-3108-A3) PB-24 (Through STA-3108-D1)
Cables:	CAB-1284CC (IEEE-1284C standard shielded cable with 18 twisted pairs, used for analog and digital connections to 3108)

B
Glossary

2's complement
A number in the base-2 (binary) system that is the true complement of another number. A 2's complement is usually derived by reversing the digits in a binary number (changing 1s to 0s and 0s to 1s) and adding 1 to the result. When 2's complements are used to represent negative numbers, the most significant (leftmost) digit is always 1.

About-trigger acquisition mode
A data acquisition triggering mode in which the data acquisition is started by an internal or external trigger, then continues after a trigger event until a specified number of samples has been acquired. *See also* Trigger (data acquisition) *and* Trigger modes.

Absolute accuracy
A measure of the uncertainty of an instrument reading compared to that of a primary standard having absolute traceability to the National Institute of Standards and Technology. Accuracy is often separated into gain and offset terms. *See also* Rated accuracy.

Active edge
The positive, rising edge of a trigger signal or the negative, falling edge. Data acquisition systems typically may be configured to interpret specifically a positive edge or specifically a negative edge, as a trigger event. *See also* Trigger (data acquisition) *and* Trigger polarity.

Acquisition time
In general, the minimum amount of time that an analog signal must be present at the input of an analog-to-digital (A/D) converter for an A/D conversion to take place. For a sampling A/D converter, which contains a sample-and-hold (SH) front end, the acquisition time specifies the time that the analog signal must be present at the SH front end before the A/D conversion starts. Acquisition time is also referred to as Aperture time and Sample window. *See also* Analog-to-digital converter, Sampling analog-to-digital converter, Sample-and-hold.

A/D converter
See Analog-to-digital converter.

ADC
See Analog-to-digital converter.

Address
A number specifying a location in memory where data is stored.

Analog-to-digital converter
An electronic device, often an integrated circuit, that converts an analog voltage to a digital value. All digital instruments use analog-to-digital converters to convert the input signals into digital information. Sometimes called an A/D converter or an ADC.

Analog trigger
An event that occurs at a user-selected point on an analog input signal. The polarity, sensitivity, and hysteresis of the analog trigger can often be programmed. S*ee also* Trigger (data acquisition), Trigger conditions, Trigger hysteresis, Trigger mode, Trigger polarity, Trigger sensitivity.

Aperture delay
The time delay between when an analog-to-digital converter receives a conversion command and when it starts the conversion process. *See also* Analog-to-digital converter, aperture jitter.

Aperture time
See acquisition time.

Aperture jitter
The short-term variation of aperture delay. Also called Aperture uncertainty. *See also* Aperture delay.

Aperture uncertainty
See aperture jitter.

API
See Application Programming Interface.

Application programming interface
A set of routines used by an application program to direct the performance of a procedure by the computer's operating system.

Base address
An I/O address that is the starting address for programmable registers. All subsequent registers are accessed by adding to the base address.

Bias current (in differential amplifier)
A small but finite current drawn through an input terminal of a differential amplifier to the corresponding input transistor. Depending on the design of the amplifier, the bias current flows into the base of a bipolar transistor, the gate of a junction field effect transistor, or the biased protective diodes in front of a MOS field effect transistor. Ideally, the bias current through the input-high terminal of the amplifier is identical to the bias current through the input-low terminal. Because bias currents flow through the resistance of the signal source and through the resistance between the signal source and ground, compensation techniques are sometimes employed to minimize input errors caused by the resulting voltage drops.

Bipolar
An analog signal range that includes both positive and negative values.

Burst clock
For a data acquisition board operating in the burst mode, a pulse-emitting circuit that determines the analog data conversion rate. *See also* Burst conversion mode *and* Conversion rate.

Burst clock rate
The rate at which timing pulses are emitted from a pacer clock. *See also* Burst clock, Burst conversion mode.

Burst clock frequency
See burst clock rate.

Burst conversion mode
A data acquisition mode in which a group of analog input channels are scanned at a rate determined by the pacer clock and each channel within the group is converted at a higher rate determined by the burst clock. This mode minimizes the skew between channels. *See also* Burst clock, Pacer clock.

Bus mastering
On a microcomputer bus such as the PCI bus, the ability of an expansion board to take control of the bus and transfer data to memory at high speed, independently of the CPU. Replaces direct memory access (DMA).

Bus
An interconnection system that allows each part of a computer to communicate with the other parts.

Byte
A group of eight bits.

Channel
On a data acquisition board, one of several input or output paths on the board. Multiple analog input channels are commonly connected to one analog-to-digital converter, one at a time, using a multiplexer. *See also* Multiplexer *and* Analog-to-digital converter.

Channel-gain queue
A user-defined scan sequence in a data acquisition device. It specifies both the position in the sequence and the gain at which an analog input channel is scanned — or, in some cases, the output range at which an analog output channel is updated. It can also specify whether the input or output mode is bipolar or unipolar and whether the input mode is single-ended or differential. *See also* Channel *and* Scan (data acquisition).

CMRR
See Common Mode Rejection Ratio (CMRR).

Cold junction
The junction in a thermocouple circuit that is held at a stable, known temperature. Also known as a reference junction.

Cold-junction compensation (CJC)
A method of compensating for ambient temperature variations in thermocouple circuits.

Common Mode Rejection Ratio (CMRR)
The ability of a differential input to reject interference from a voltage common to both its input terminals with respect to ground—the common mode voltage. Numerically,

$$\text{CMRR} = \frac{\text{Common mode voltage}}{\text{Common mode error, the part of common mode voltage not rejected}}$$

The CMRR is usually expressed in decibels [i.e. as $20\log_{10}(\text{CMRR})$], at a specified frequency. *See also* Common mode voltage *and* Differential input.

Common mode voltage
A voltage between input low and chassis ground of an instrument. A differential input "sees" the common mode voltage as a common component of the voltages at both the input-high and input-low terminals and rejects all but a small fraction. *See also* Common Mode Rejection Ratio (CMRR) *and* Differential input.

Contact bounce
The intermittent and undesired opening of relay contacts during closure, or the intermittent and undesired closing of relay contacts during opening.

Conversion rate
The rate at which sampled analog data is converted to digital data or at which digital data is converted to analog data.

Conversion time
The time required to complete an analog-to-digital conversion or a digital-to-analog conversion.

Crosstalk
The coupling of a signal from one input to another (or from one channel to another channel or to the output) by conduction or radiation. Crosstalk is expressed in decibels at a specified load and up to a specific frequency.

D/A converter
See Digital-to-analog converter.

DAC
See Digital-to-analog converter.

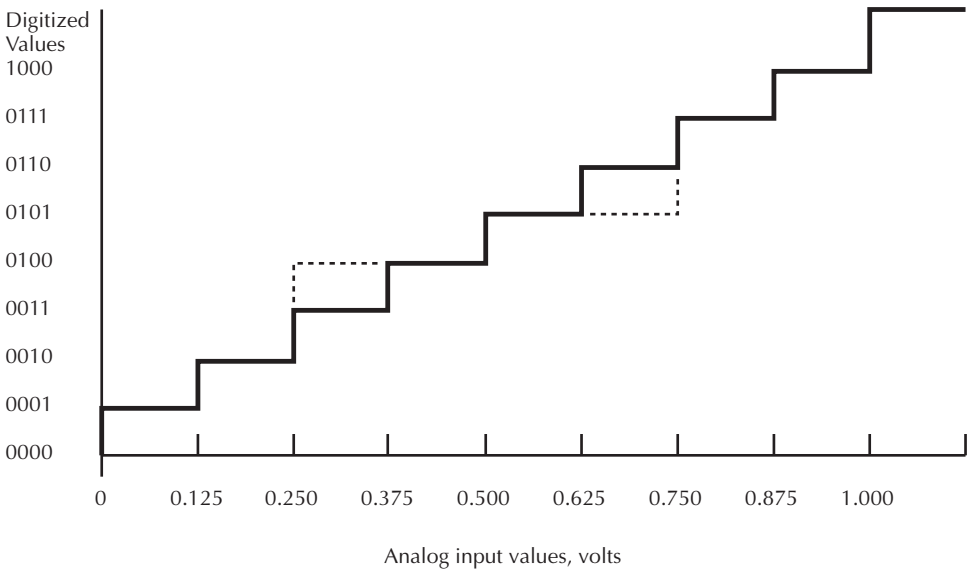
Darlington
A high-gain current amplifier composed of two bipolar transistors, typically integrated in a single package.

Differential amplifier
An amplifier that measures the difference between the voltages at two input terminals, input-high and input-low, each of which is referenced to a common ground. A differential amplifier rejects the common mode voltage—the common voltage relative to ground, as measured at the input low terminal—to an extent limited by the common-mode rejection ratio of the amplifier.

Differential input
An analog input circuit that measures the difference between the voltages at two input terminals—input high and input low, each of which is referenced to a common ground. A differential input rejects the common mode voltage—the common voltage relative to ground, as measured at the input low terminal—to an extent limited by the common-mode rejection ratio of the circuit. *See also* Common mode voltage, Common-mode rejection ratio (CMRR) *and* Single-ended input.

Differential linearity
See Differential Nonlinearity (DNL).

Differential Nonlinearity (DNL)
The maximum deviation of a real digitized step width or height from the ideal digitized step width or height. The input range of a data acquisition board is divided into a series of discrete steps, each step ideally having a height of one least significant bit (LSB). For a 4 bit analog-to-digital converter, the solid curve below illustrates ideal digitized steps over an entire 1 V input range, resulting in a differential nonlinearity of 0 LSB. The dashed curve illustrates deviations from ideality resulting in a differential nonlinearity of ±1.0 LSB. *See also* Least Significant Bit (LSB) and Analog-to-digital converter.



Digital-to-analog converter
A device that translates digital data to an analog signal. A digital-to-analog converter takes a succession of discrete digital values as input and creates an analog signal whose amplitude, moment by moment, corresponds to each digital value. *Compare* Analog to digital converter.

Digital trigger
An event that occurs at a user-selected point on a digital input signal. The polarity and sensitivity of the digital trigger can often be programmed. *See also* trigger, trigger conditions, trigger polarity, *and* trigger sensitivity.

DLL
See Dynamic Link Library.

DMA (Direct Memory Access) channels
ISA bus PCs offer eight parallel channels for DMA mode data transfers. Several of these are reserved for exclusive use by the computer. The remainder are available for use by user-supplied I/O options, such as plug-in data acquisition cards. Also called DMA levels. *See also* DMA mode.

DMA (Direct Memory Access) levels
See DMA (Direct Memory Access) channels.

DMA (Direct Memory Access) mode
A mode in which data transfers directly between an I/O device and computer memory, bypassing the CPU. In the most general sense, PCI bus mastering is a DMA mode. More commonly, however, DMA mode refers to data transfers across the ISA bus, using special circuitry on the computer motherboard. *See also* Bus mastering.

Direct Memory Access (DMA)
See DMA (Direct Memory Access) mode.

DNL
See Differential Nonlinearity.

Drift
A gradual change of a reading or an amplifier output over time with no changes in the input signal or operating conditions.

Driver
Software that controls a specific hardware device, such as a data acquisition board.

Dynamic Link Library (DLL)
A software module in Microsoft Windows containing executable code and data that can be called or used by Windows applications or other DLLs. DLL functions and data are loaded and linked at run time when they are referenced by a Windows application or other DLLs.

Expansion slot
A socket in a computer designed to hold expansion boards and connect them to the system bus (data pathway).

External pacer clock source
A source of pulses that is connected externally to a data acquisition board and is used to pace or time events such as analog-to-digital conversions, digital-to-analog conversions, data sampling, interrupt generation, digital I/O transfers, etc.

External trigger
An analog or digital hardware event from an external source that starts an operation. *See also* Internal trigger.

Floating
Refers to a signal source that is either totally ungrounded (a battery, for example) or is not connected either directly or indirectly to the building ground or analog signal ground. (Real floating signal devices do have a finite, though very small, coupling to ground due to finite insulation resistance and other sources of current leakage.)

Foreground task
An operation, such as a task that occurs in the single or synchronous mode, that cannot take place while another program or routine is running.

Field-Programmable Gate Array (FPGA)
A gate array in which the logic network can be programmed into the device after its manufacture. An FPGA consists of an array of logic elements, either gates or lookup table RAMs, flip-flops, and programmable interconnect wiring. Most FPGAs are reprogrammable, because their logic functions and interconnects are defined by RAM cells. Others can only be programmed once, by closing "antifuses," and retain their programming permanently. In one type, part of the array can be reprogrammed while other parts are active.

FPGA designs are prepared using CAD software tools, usually provided by the chip vendor, to do technology mapping, partitioning and placement, routing, and binary output. The resulting binary can be programmed into a ROM connected to the FPGA or downloaded from a computer connected to the FPGA.

FIFO
First-In/First-Out memory buffer. The first data into the buffer is the first data out of the buffer. On a data acquisition board, a FIFO allows data collection to continue while the board waits for data transfer access to the host computer.

FPGA
See Field-Programmable Gate Array (FPGA).

Gain
The factor by which an incoming signal is multiplied by an amplifier.

Gate (signal)
A signal that in the active state enables an operation and in the inactive state inhibits the operation.

Glitch energy
A glitch is an unwanted transient superimposed on the output of a digital-to-analog converter. Glitch energy is a measure of this transient. A simple figure of merit is an integral of the transient voltage with time. Also called glitch charge or glitch impulse.

GPIB
Abbreviation for General Purpose Interface Bus, also referred to as the IEEE-488 bus. It is a standard for parallel interfaces.

Ground loop
A current loop created when a signal source and a signal measurement device are grounded at two separate points on a ground bus through which noise currents and/or currents from other devices flow. Due to the finite resistance of the bus, these currents generate voltage drops between the two ground connection points, which can cause errors and noise in the signal measurement.

IEEE-488
See GPIB.

Input bias current
The current that flows at the input of an analog measurement circuit due to internal circuitry and bias voltage. Also, at conditions of zero input signal and offset voltage, the current that must be supplied to the input-high measuring terminal to reduce the output indication to zero. The input bias current is drawn through the source resistance of a signal source. Therefore, in critical and/or low-level measurements, bias current compensation or attention to source resistance may be required to minimize errors.

Input/Output (I/O)
The process of transferring data to and from a computer-controlled system using its communication channels, operator interface devices, data acquisition devices, or control interfaces. Also refers to the electrical inputs and outputs for data signals. For example, one may say that a data acquisition board provides both "digital and analog I/O," meaning "digital and analog inputs and outputs."

Input/output port
A channel through which data is transferred between an input or output device and the processor.

Instrumentation amplifier
A high-performance differential amplifier having high input impedance at both the input high and input low terminals and typically characterized by high common mode rejection ratio (CMRR) and low drift. An instrumentation amplifier normally operates either at a fixed gain or, in the case of a Programmable Gain Instrumentation Amplifier (PGIA at a gain set using a digital control signal. *See also* Differential amplifier, Differential input, Drift, Common Mode Rejection Ratio (CMRR).

Internal pacer clock
See Pacer clock.

Integral linearity
See Linearity.

Internal trigger
A software-generated event that starts an operation. *See also* External trigger.

Interrupt
For a data acquisition board, a signal to the CPU indicating that the board detected a condition or event calling for special processing. An interrupt causes the CPU to temporarily stop the current processing task, complete the special processing task, and then return to the original processing task. *See also* Interrupt level, Interrupt-mode operation, Interrupt Service Routine (ISR).

Interrupt level
A specific priority that ensures that high priority interrupts are serviced before low priority interrupts.

Interrupt-mode operation
Mode in which a data acquisition board acquires or generates samples using an Interrupt Service Routine (ISR).

Interrupt Service Routine (ISR)
A software program that handles interrupts.

ISA Bus
Industry Standard Architecture. A 16-bit wide bus architecture used in most MS-DOS and Windows computers. Sometimes called the AT bus.

Least Significant Bit (LSB)
The lowest order bit, usually the rightmost bit, in the binary representation of a digital quantity. Measurement precision or accuracy is sometimes specified in terms of *multiple* Least Significant Bits (LSBs). In that case, the precision or accuracy is represented by the binary number that results from *counting* the specified number of least significant bits. For example, the binary number that results from counting 3 LSBs is 0011 (0001 + 0001 + 0001 = 0011). Therefore, a 12-bit number precise to within 3 LSBs is precise to within (0011)/(1111 1111 1111) = 3/4096 = 0.07% of full scale.

Linearity
For a curve relating instrument readings to known inputs, the maximum deviation of readings from a straight line drawn between readings at zero and full range.

LSB
See Least Significant Bit.

Map
Any representation of the structure of an object. For example, a memory map describes the layout of objects in an area of memory, and a symbol map lists the association between symbol names and memory addresses in a program.

Multiplexing
A technique whereby multiple signals are sent to one input, one signal at a time in a specified sequence.

Multiplexer (MUX)
A circuit that switches multiple signals into one input, one signal at a time in a specified sequence.

MUX
See Multiplexer.

Negative-edge triggering
Digital trigger mode in which the triggering action starts on the falling edge of the signal. *See also* Trigger polarity *and* Digital trigger.

Noise
An undesirable electrical signal from an external source such as an AC power line, motors, generators, transformers, fluorescent lights, CRT displays, computers, and radio transmitters.

OCX
Abbreviation for OLE Custom Control. Also referred to as ActiveX control.

Offset, voltage (data acquisition)
An error voltage that appears in series with an analog input terminal of a data acquisition board and is generated by the input circuits of the board.

Paced mode
A data-acquisition analog-to-digital conversion mode in which one sample is converted following each pulse of a pacer clock. That is, the conversion rate equals the pacer clock rate. *See also* Pacer clock, Conversion rate, Sample rate, and Analog-to-digital converter.

Pacer clock
An internal (on-board) or external clock that emits pulses that are used to pace or time events such as analog-to-digital conversions, digital-to-analog conversions, data sampling, interrupt generation, digital I/O transfers, etc.

p-p
See peak-to-peak.

Peak
The highest magnitude, either positive or negative. For a signal that is symmetrical about zero, peak = ½. *See also* peak-to-peak.

Peak-to-peak
The difference between the minimum value and maximum value of an alternating signal.

Pacer clock rate
The rate at which timing pulses are emitted from a pacer clock. *See also* Pacer clock *and* Paced mode.

Pass-through mode
See Target mode.

PCI
Abbreviation for Peripheral Component Interconnect. It is a standard for a local bus.

PGIA
See Instrumentation amplifier.

Plug and Play
A set of specifications developed by Intel that allows a PC to configure itself automatically to work with peripherals such as monitors, modems, and printers. A user can "plug" in a peripheral and "play" it without manually configuring the system. A Plug and Play PC requires both a BIOS that supports Plug and Play and a Plug and Play expansion card.

PnP
See Plug and Play.

Port
See input/output port.

Polarity mode
The mode that specifies whether a data acquisition channel inputs or outputs both positive and negative signals (bipolar mode) or only positive signals (unipolar mode) relative to analog ground. *See also* Bipolar *and* Unipolar.

Port group
For digital I/O emulating the I/O of an 8255 programmable peripheral interface chip, a group of three 8 bit ports, commonly labeled PA, PB, and PC. Digital I/O that emulates multiple 8255 chips is typically divided into multiple port groups.

Port I/O call
A software program statement that assigns bit values to an I/O port or retrieves bit values from an I/O port. Examples include a C/C++ statement containing an `inp` or `outp` function or a Basic statement containing a `peek` or `poke` function.

Positive-edge triggering
A digital trigger mode in which the triggering action starts on the rising edge of the signal. *See also* Trigger polarity, Digital trigger.

Post-trigger acquisition mode
A data acquisition triggering mode in which the data acquisition starts after an internal or external trigger event and continues until a specified number of samples has been acquired or until the operation is stopped by software. *See also* Trigger (data acquisition) *and* Trigger modes.

Pre-trigger acquisition mode
A data acquisition triggering mode in which the data acquisition is started before an internal or external trigger occurs. *See also* Trigger (data acquisition), Trigger modes.

Programmable Gain Instrumentation Amplifier (PGIA)
See Instrumentation amplifier.

Pseudo-Simultaneous Sample and Hold
Emulating Simultaneous Sample and Hold (SSH) by scanning a group of data acquisition channels at the highest practical rate while repeating scans at a much slower rate. This is commonly done in the burst data-conversion mode, by running the burst clock at a rate close to maximum throughput while running the pacer clock at a much slower rate. Typically used when multiple parameters must be compared at essentially the same instant in time but slight timing variations are acceptable. *See also* Burst clock, Burst conversion mode, Pacer clock, Simultaneous Sample and Hold (SSH), Scan (data acquisition), Throughput.

Pseudo-SSH
See Pseudo-Simultaneous Sample and Hold.

Pulse duration
See Pulse width.

Pulse width
The time interval between the rising and falling edges of a pulse, specified at a certain percentage of the peak amplitude—commonly 50% for a rectangular pulse. Also referred to as pulse duration.

QRAM
Queue RAM. Onboard memory on a data acquisition board that holds information about the channel number and gain, and sometimes other settings, for each position in the channel-gain queue. *See also* Channel-gain queue.

Range
A continuous band of signal values that can be measured or sourced. In bipolar instruments, range includes positive and negative values.

Rated accuracy
The limit that errors will not exceed when an instrument is used under specified operating conditions. It is expressed as a percentage (of input or output) plus a number of counts. *See also* Absolute accuracy.

Register
A set of bits of high-speed memory within a microprocessor or other electronic device used to hold data for a particular purpose.

Resolution
The smallest increment of a signal that can be measured, sourced, or displayed. Also called sensitivity or minimum resolvable quantity. For a digitized signal, resolution is typically expressed in bits or digits. By contrast, sensitivity is expressed in engineering units.

Ringing (in digital-to-analog converter)
A transient oscillation in the output of a Digital-to-Analog Converter (DAC) that follows an abrupt change in input, analogous to the decaying vibrations of a clapped bell. Susceptibility to ringing in a DAC is caused by excessive capacitance in the driven load.

rms (or RMS)
See Root-mean-square (rms).

Root-mean-square (rms)
The rms value of an alternating signal equals the square root of the time average of the square of that signal. A sinusoidal alternating current having a particular rms value and a DC current having that same value produce the same joule heating when connected to a given resistor. Sometimes referred to by standard deviation.

S
Abbreviation for the Sample or Samples unit. *See* Sample (data acquisition).

Sample (data acquisition)
A single value that is read from or written to one channel. *See also* Channel.

Sample and Hold (SH)
An operation, or electronic circuit, in which an analog input signal is stored briefly as a voltage on a capacitor, typically until it can be digitized by an analog-to-digital converter. *See also* Simultaneous sample and hold *and* Analog-to-digital converter.

Sample rate
The rate at which a continuous-time signal is sampled. The sample rate is frequently expressed in units of samples/second (S/s), kilosamples/second (kS/s), or megasamples/second (MS/s).

Sampling analog-to-digital converter
An analog-to-digital converter containing a sample-and-hold circuit at the front end, which captures the incoming analog signal and holds it for the duration of the analog-to-digital conversion process. *See also* Analog-to digital converter, Sample-and-Hold (SH).

Saturation (amplifier)
Amplifier condition in which an increase of the input signal produces no further increase in the output signal.

Scan (data acquisition)
To sample a group of input channels once at a specified acquisition rate, either in numerical sequence or in the sequence specified in a channel-gain queue. *See also* Channel-gain queue.

Scan rate
The rate at which a group of channels is sampled, measured from the start of one scan to the start of the next scan.

Scatter-gather
A very high speed, direct memory access data transfer method under PCI bus mastering. Data written to memory may be "scattered" into noncontiguous memory blocks. When reading data, the memory block locations are first supplied to the bus master, and then data is rapidly "gathered" from the noncontiguous memory blocks.

Settling time (data acquisition)
The time needed for the output of a digital-to-analog converter or a combined input amplifier/analog-to-digital converter to stabilize, within a specified error, following an abrupt change in input.

SH
See Sample and Hold.

Shielding
A metal enclosure for a circuit being measured or a metal sleeve surrounding wire conductors to lessen interference, interaction, or current leakage. The shield is usually grounded.

Simultaneous Sample and Hold (SSH)
An operation, or electronic circuit, in which multiple analog input signals are simultaneously sampled and stored, typically as voltages on capacitors, until sequentially read by a scanning analog-to-digital converter system. *See also* Analog-to-digital converter. Typically used when multiple parameters must be compared at exactly the same instant in time.

Single-ended input (data acquisition)
An analog input circuit that measures the voltage at one input terminal relative to a common ground. *See also* Differential input.

Software trigger
A programmed event that starts an operation such as data acquisition.

SSH
See Simultaneous Sample and Hold (SSH).

Strobe
A timing signal that initiates and coordinates the passage of data, typically through an input or output device interface.

Target mode
A PCI bus mode in which data from a data acquisition board is transferred indirectly to the computer memory in the foreground, via the host computer CPU, instead of directly, via Bus mastering. Sometimes referred to as pass-through operation. *See also* bus mastering and foreground task.

Temperature coefficient
A change in the value of a measured or sourced signal with a change in temperature. The temperature coefficient is commonly expressed as an absolute or relative change—or both—per degree C or degree F.

Termination mode
Refers to the mode in which a user connects signals to the multiplexer—and, internally, to the differential amplifier—of a data acquisition board. The choices are single-ended mode or differential mode. *See also* Single-ended input (data acquisition), Differential input.

Thermal emfs
Temperature-dependent voltages that develop across junctions of dissimilar metals. In an ideal measurement circuit, all such junctions would be wired to high and low differential inputs as identical pairs at identical temperatures, resulting in cancellation of the thermal emfs. Practically, however, temperature differences across the circuit and imperfect metal-to-metal junctions result in net voltage errors, which must be minimized when measuring low-level signals.

Throughput
The maximum rate at which a data conversion system can perform repetitive conversions within a specified accuracy. It is determined by summing the various times required for each part of the conversion system and then calculating the inverse of this time. The throughput rate takes into account the total time required to process a signal and store the value in either on-board or system memory.

Trap (*verb)*
To intercept an action or event before it occurs, usually in order to do something else. Trapping is commonly used by debuggers to allow interruption of program execution at a given spot.

Trigger conditions
Refers to trigger sensitivity, polarity, etc.

Trigger (data acquisition)
An event that starts or stops an operation. A trigger can be a specific analog, digital, or software condition. *See also* analog trigger *and* digital trigger.

Trigger hysteresis
Applies only to analog triggers. A specified voltage change, opposite in polarity to the trigger polarity, through which an analog trigger signal must move before triggering can occur. For positive-edge triggering to occur, the signal must first fall below the specified trigger voltage by at least the amount of the hysteresis value. For negative-edge triggering to occur, the signal must rise above the specified trigger voltage level by at least the amount of the hysteresis value. Trigger hysteresis helps prevent false triggering due to noise. *See also* Analog trigger, Trigger polarity.

Trigger jitter
The short-term variation in trigger latency. *See also* Trigger latency.

Trigger latency
The fixed time offset between the trigger event and the first sample point.

Trigger mode
Refers to when data acquisition begins and ends in relationship to the trigger. Trigger modes include normal-trigger, pre-trigger, about-trigger, post-trigger, trigger-to-trigger, and trigger-to-about-trigger. *See also* Pre-trigger acquisition mode, About-trigger acquisition mode, Post-trigger acquisition mode.

Trigger polarity
For edge-sensitive triggers, trigger polarity defines whether the trigger occurs when the signal is rising (positive direction) or when the signal is falling (negative direction). For level-sensitive triggers, trigger polarity defines whether the trigger occurs when the signal is above a level (positive) or below a level (negative).

Trigger sensitivity
Refers to the edge and/or level of a trigger. For analog triggers, trigger sensitivity defines whether the trigger occurs on a transition across a specified value (edge) or whether the trigger occurs when it is above or below a specified value (level). For digital triggers, trigger sensitivity defines whether the trigger occurs on a transition from one state to another state (edge) or whether the trigger occurs when it is at a specified value (level).

TTL
Abbreviation for Transistor-Transistor-Logic. A popular logic circuit family that uses multiple-emitter transistors. A low signal state is defined as a signal 0.8V and below. A high signal state is defined as a signal +2.0V and above.

Unipolar
An analog signal range that is always positive (above zero).

Sources:
Howe, Denis, editor, *The Free On-line Dictionary of Computing*, http://wombat.doc.ic.ac.uk/

Keithley Instruments, Inc. technical staff and Keithley *Catalog and Reference Guide* (full line catalog), glossary, 1998

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